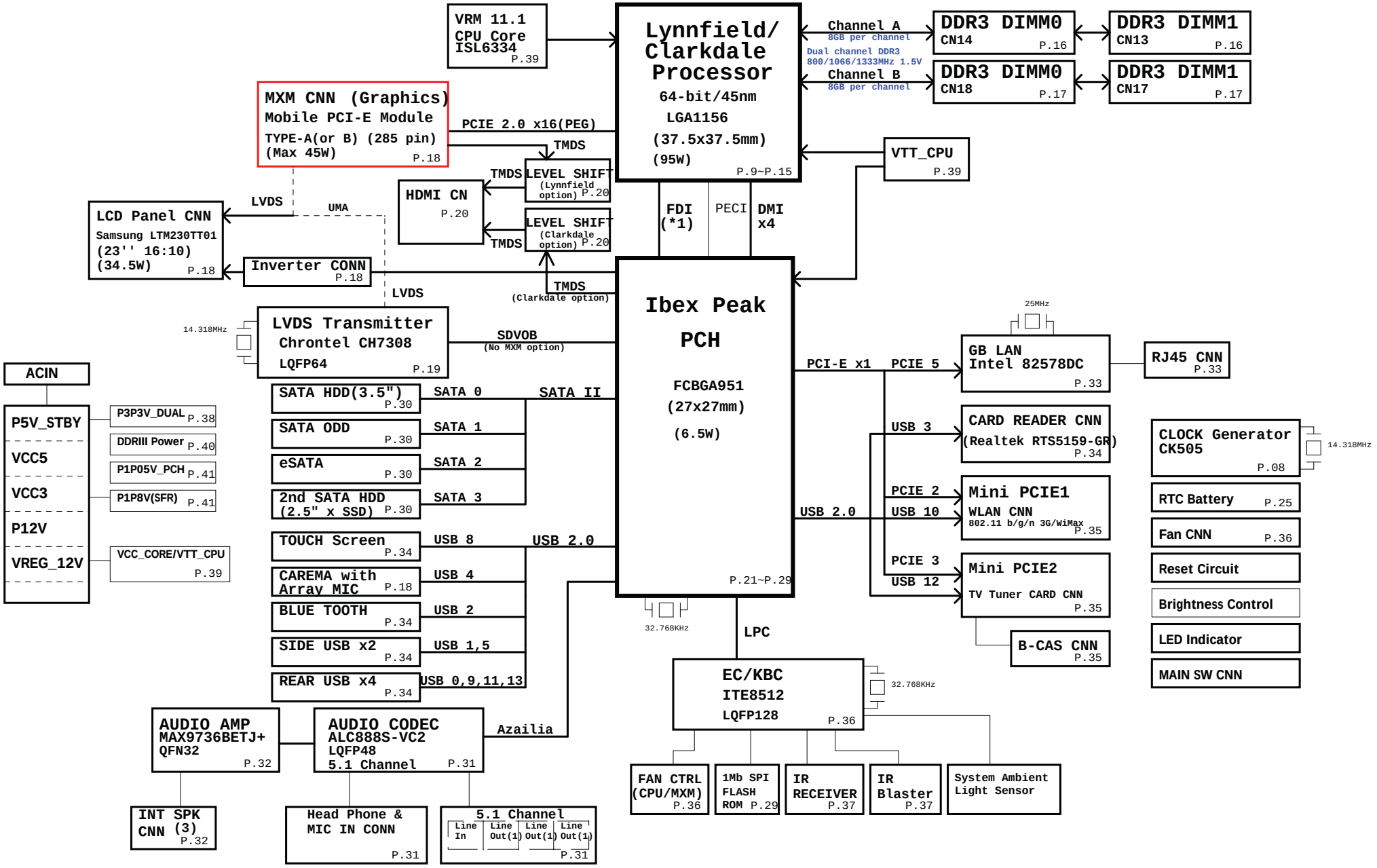
EL5 Block Diagram :



FDI - Used only for the Clarkdale processor.

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Title: BLOCK DIAGRAM		
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Net name Description :

Voltage Rails

P5V_STBY	5.0V always on power rail by LATCH or ACIN
P3P3V_STBY	3.3V always on power rail by LATCH or ACIN
P1P5V	1.5V switched power rail by SUSB#/PM_SLP_S3#
P2P5V	2.5V switched power rail by SUSB#/PM_SLP_S3#
VCC3	3.3V switched power rail by SUSB#/PM_SLP_S3#
VCC5	5.0V switched power rail by SUSB#/PM_SLP_S3#
P12V	12V switched power rail by SUSB#/PM_SLP_S3#
VREG_12V	12V switched power rail for CPU Vcore
VCCP	Core Voltage for CPU
P1V1_CPU_VTT	1.1V power rail for AGTL+ termination & PCH DMI I/F by SUSB#/PM_SLP_S3#
P1P05V_PCH	1.05V power rail for PCH Core;PCH I/O;DMI;PCIE;SATA by SUSB#/PM_SLP_S3#
P1P8_SFR	1.8V power rail for CPU PLL & PCH NAND I/F by SUSC#/PM_SLP_S4#
P1P5V_SUS	1.5V power rail for DDRIII by SUSC#/PM_SLP_S4#
0.75VDDT_DDR3	0.75V DDRIII Termination Voltage by SUSB#/PM_SLP_S3#

Part Naming Conventions

C = Capacitor
CN = Connector
D = Diode
F = Fuse
L = Inductor
Q = Transistor
R = Resistor
RP = Resistor Pack
U = Arbitrary Logic Device
Y = Crystal and Osc

Net Name Suffix

or _N = Active Low signal

Board Stack up Description

02

PCB Layers

Layer 1	Component Side, Microstrip signal Layer
Layer 2	Power Plane
Layer 3	Normal Signal / Ground 1 Plane
Layer 4	Stripline Layer(High Speed)
Layer 5	Ground Plane
Layer 6	Solder Side,Microstrip signal Layer

Layers : 6 Depth 1.2mm Impence 55 ohms +/- 10%

	Single End Impedance	Differential Impedance for Microstrip	Differential Impedance for Stripline
Host Clock	55 ohm +/- 15%	95 ohm +/- 15%	100 ohm +/- 15%
SRC Clock	55 ohm +/- 15%	95 ohm +/- 15%	100 ohm +/- 15%
Host Bus	55 ohm +/- 15%		
DDR3 CLK	42 ohm +/- 15%	70 ohm +/- 20%	70 ohm +/- 20%
DDR3 Strobe	55 ohm +/- 15%		85 ohm +/- 20%
DDR3 Bus	55 ohm +/- 15%		
DMI Bus	55 ohm +/- 15%	95 ohm +/- 15%	100 ohm +/- 15%
PCIE Bus	55 ohm +/- 15%	95 ohm +/- 15%	100 ohm +/- 15%
SATA		95 ohm +/- 15%	100 ohm +/- 15%
SDVO	55 ohm +/- 15%	95 ohm +/- 15%	100 ohm +/- 15%
LVDS		100 ohm +/- 15%	100 ohm +/- 15%
USB		90 ohm +/- 15%	90 ohm +/- 15%
Lan	50 ohm +/- 15%		

For no M3 support with Intel LAN:

-1.05 V ME powered by 1.05 V PCH
-3.3 V SPI (3.3 V EPW) powered by 3.3 V Main
-VCCLAN (LAN MAC well) is powered by 1.05 ME well (which is powered by 1.05 PCH)
-VCCLANPHY power is gated by SLP_LAN#

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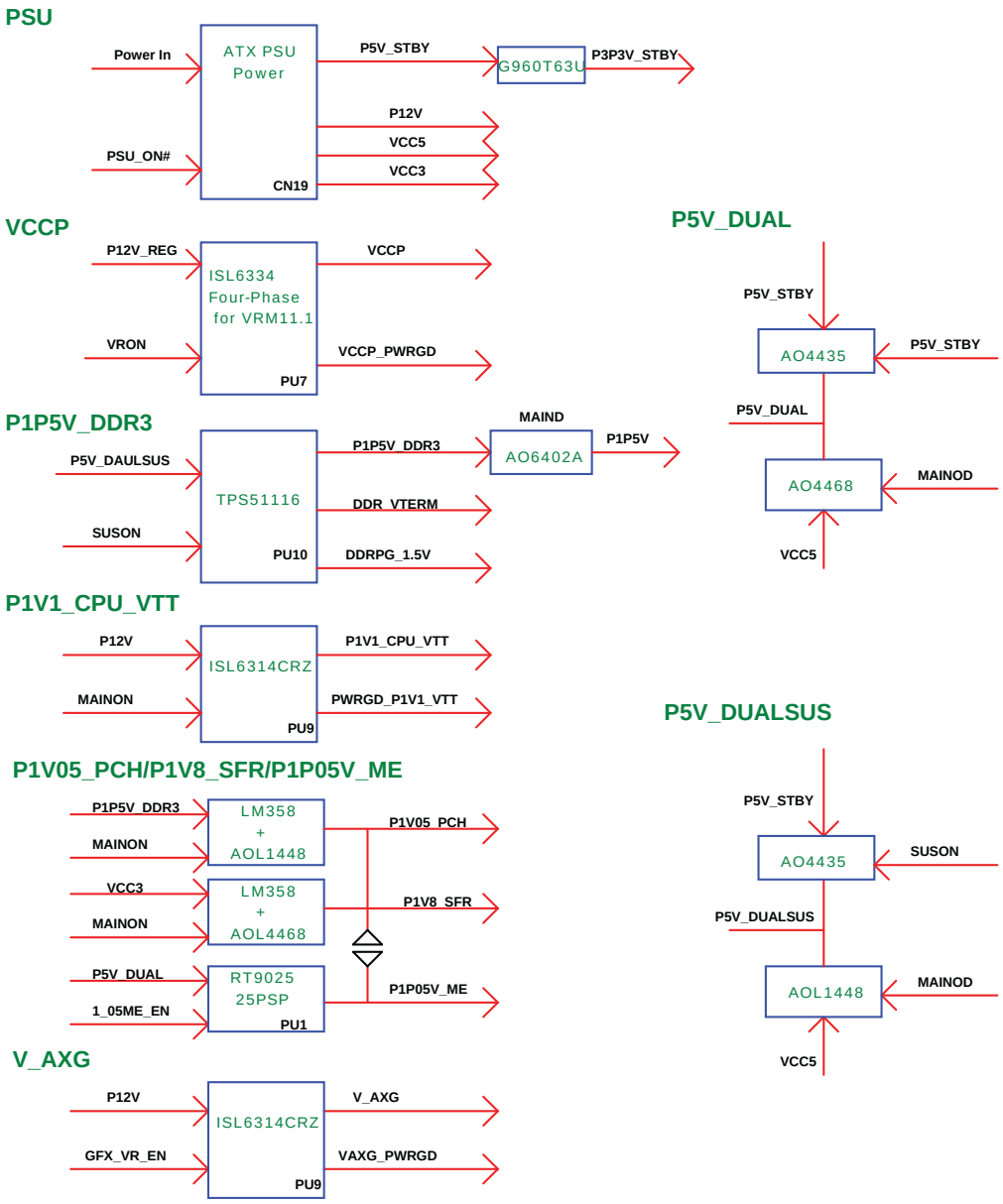
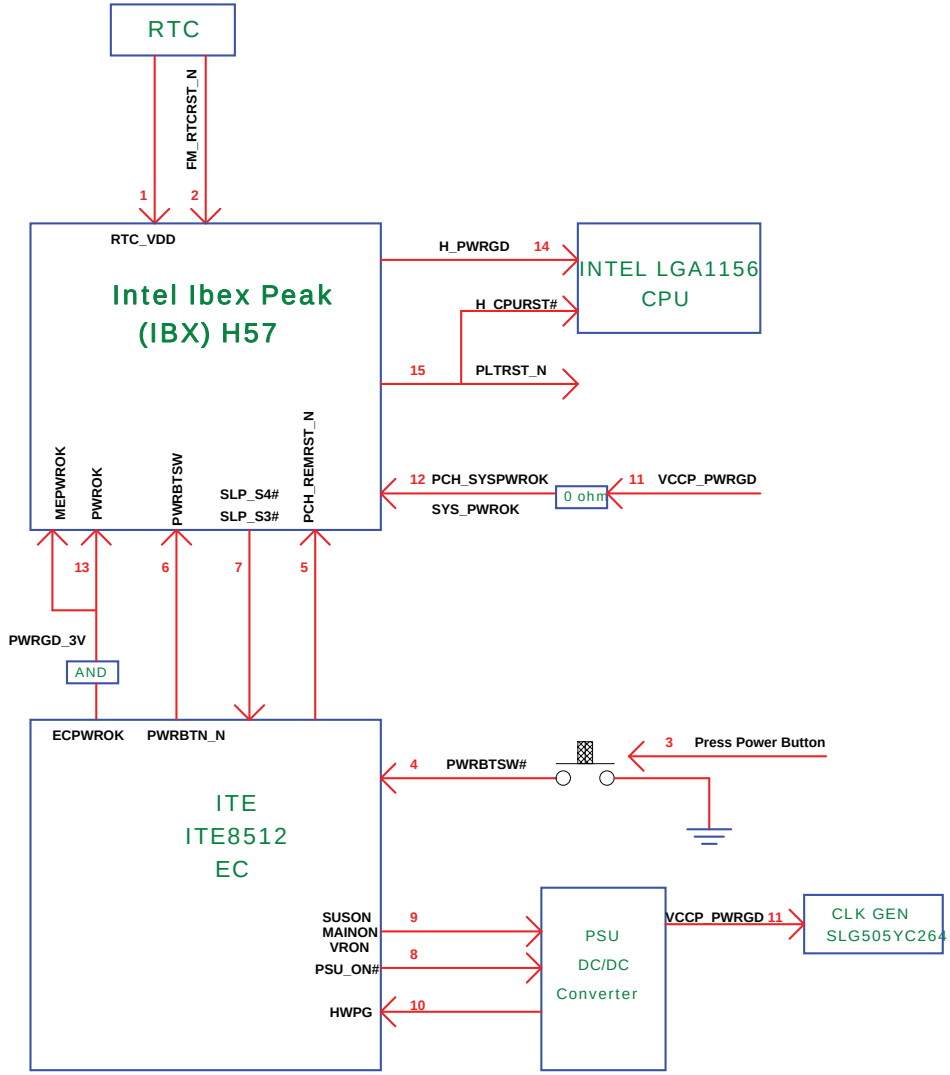
Power rail control



Power on Sequence



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Title: Timing Diagram
Size: Custom | Document Number: ELS | Rev: A02
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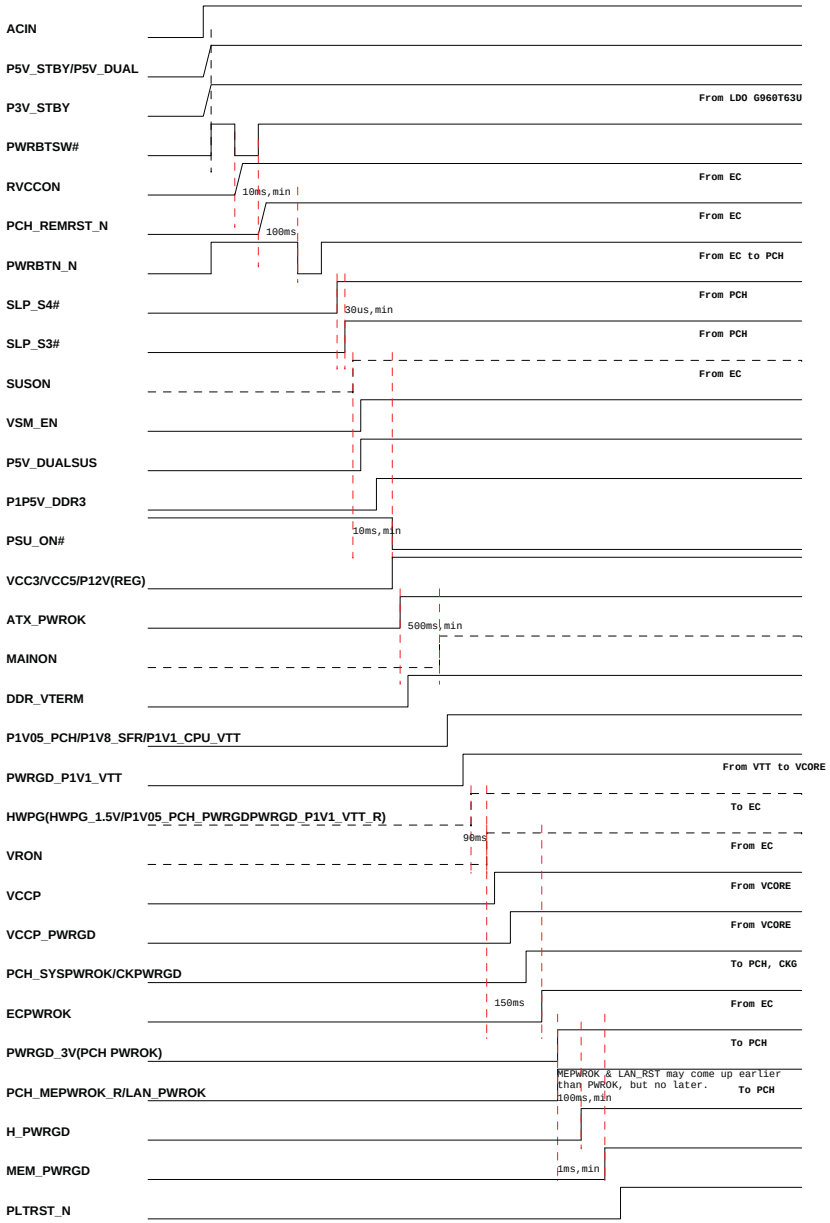
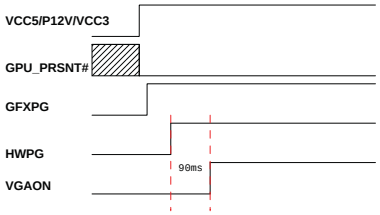
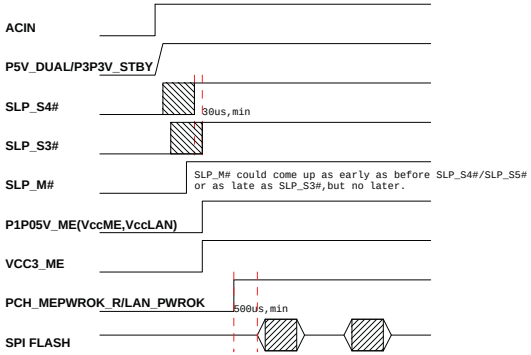
Power on Sequence :



MXM POWER ON



SLP_M#, M3 ON



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Title: Timing Sequence		
Size: CustomEL5	Document Number	Rev: A02
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Power Rail	Destination	Voltage	S0 Current
VCC_CORE	Lynnfield : Default for initial power up	0.65V~1.4V 1.1V	90A(TDC) Max:110A
VTT_CPU	Lynnfield : Memory controller & shared cache Ibex Peak : DMI Ibex Peak : CPU_IO	1.045V~1.1V~1.155V 1.1V 1.05V~1.1V~1.16V	30A(TDC) Max: 35A 0.065A 0.001A
P1P8V(SFR)	Lynnfield : Internal processor PLL Ibex Peak : Internal PLL & VRMs Ibex Peak : Dual channel NAND I/F NVRAM : VCCQ NVRAM : VREF	1.71V~1.8V~1.89V 1.71V~1.8V~1.89V 1.71V~1.8V~1.89V	1.1A 0.196A 0.156A
P1P5V_SUS	Lynnfield : CPU I/O Voltage for DDRIII DIMM :	1.425V~1.5V~1.575V	6A
0.75VDDT_DDR3	DDRIII Terminator:	0.75V	?A
P1P05V_PCH	Ibex Peak : VccCore Ibex Peak : Vcc core I/O buffer Ibex Peak : DMI buffer voltage Ibex Peak : Intel Management Engine Ibex Peak : Display PLL A power Ibex Peak : Display PLL B power Ibex Peak : LAN	0.998V~1.05V~1.1V 0.998V~1.05V~1.1V 0.998V~1.05V~1.1V 0.998V~1.05V~1.1V 0.998V~1.05V~1.1V 0.998V~1.05V~1.1V 0.998V~1.05V~1.1V	1.629A 3.251A 0.065A 2.222A 0.075A 0.075A 0.372A
P1P5V	Mini PCIE : +1.5V(WLAN) Mini PCIE : +1.5V(TV)		
P2P5V	CH7308 : DVDD		
VCC3	Ibex Peak : I/O buffer voltage Ibex Peak : Display DAC Analog power CLK Gen.CK505 : VDD NVRAM : VCC MXM : 3V3 CH7308 : LVDD ALC888S : DVDD Mini PCIE : +3.3V(WLAN) Mini PCIE : +3.3V(TV) Bluetooth : +3.3V Media Card : +3.3V(JMB385) EC(IT8512) : VCC CAREMA	3.14V~3.3V~3.47V 3.14V~3.3V~3.47V	0.357A 0.069A
VCC5	Ibex Peak : Core well Ref. voltage MXM : 5V SATA ODD SATA HDD(2.5" x SSD) ALC888S : AVDD Audio AMP(MAX9736BETJ) : Touch Screen LCD Panel USB: x 5 ports	4.75V~5V~5.25V 5V	0.001A 2.5A
P3P3V_STBY	Ibex Peak : Intel Management Engine Ibex Peak : Suspend well I/O Buffer Ibex Peak : HD Audio controller Suspend Voltage LAN RTL8111DL : VDD IR Receiver EC(IT8512) : VSTBY SPI FLASH ROM	3.14V~3.3V~3.47V 3.14V~3.3V~3.47V 3.14V~3.3V~3.47V	0.086A 0.168A 0.006A
P5V_STBY	Ibex Peak : Suspend well Ref. Voltage	4.75V~5V~5.25V	0.001A
P12V	MXM : 12V INVERTER : Vin FAN_CPU FAN_MXM Audio AMP(MAX9736BETJ) : PVDD		

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Title		
	Power Budget	
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Schmatic Change List:

Date	Change Item Description	Note
11/13	1.PAGE25 ADD R766 SLP_S4#	
	2.PAGE29 ADD R767、R768、R769	
11/24	1.PAGE38 ADD PC179、PR157	
11/26	1.PAGE9 ADD C601、C602、C603、R770、R771	
11/30	1.PAGE34 ADD R772、C604	
12/01	1.PAGE18 Del R49、R53、R54、C120，Add U2、R773、R774、R775、R776、C605、C606、C607、C608、U26、Q46。For EDID	
12/03	1.PAGE41 Add PR85、PR158	
	2.PAGE19 Add PU12、PR159、PR160、PR161、PC180、PC181、PC182、PC183、PC184 For P2P5V	
	3.PAGE20 Add U25、L29、R49、R54、R55、R67、R68、R349、R681、R682、R712、R724、R725、R779、R780、R781、R782、R783、R784、R785、R786、R787、R788、R789、R790、R791、R792、R793、C19、C21、C22、C120、C609、C610、C611 for MXM HDMI Repeater	
12/04	1.PAGE18 Add C617	
VER:C		
12/22	1.PAGE18 Del U26、R774、C606、Q46、C608、R776、R773、R775、C605、C607,Add R318、R696、R314、C605。For EDID	
	2.PAGE34 Change CN33 to 5PIN CONN	
01/05	1.PAGE39 Add PR163、R800、R801。	
01/07	1.PAGE34 Del R1、R2、 Add L30。For EMI	
	2.PAGE33 ADD R802、D47。For LAN Wake up	
	3.PAGE40 PC160 connector to P1P5V_DDR3。	
01/11	1.PAGE35 Add R803、R804、R805、R806。For PCI_E detect	
	2.PAGE33 Add R807。 For LAN LED	
VER:D		

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Schmatic Change List:

Date	Change Item Description	Note

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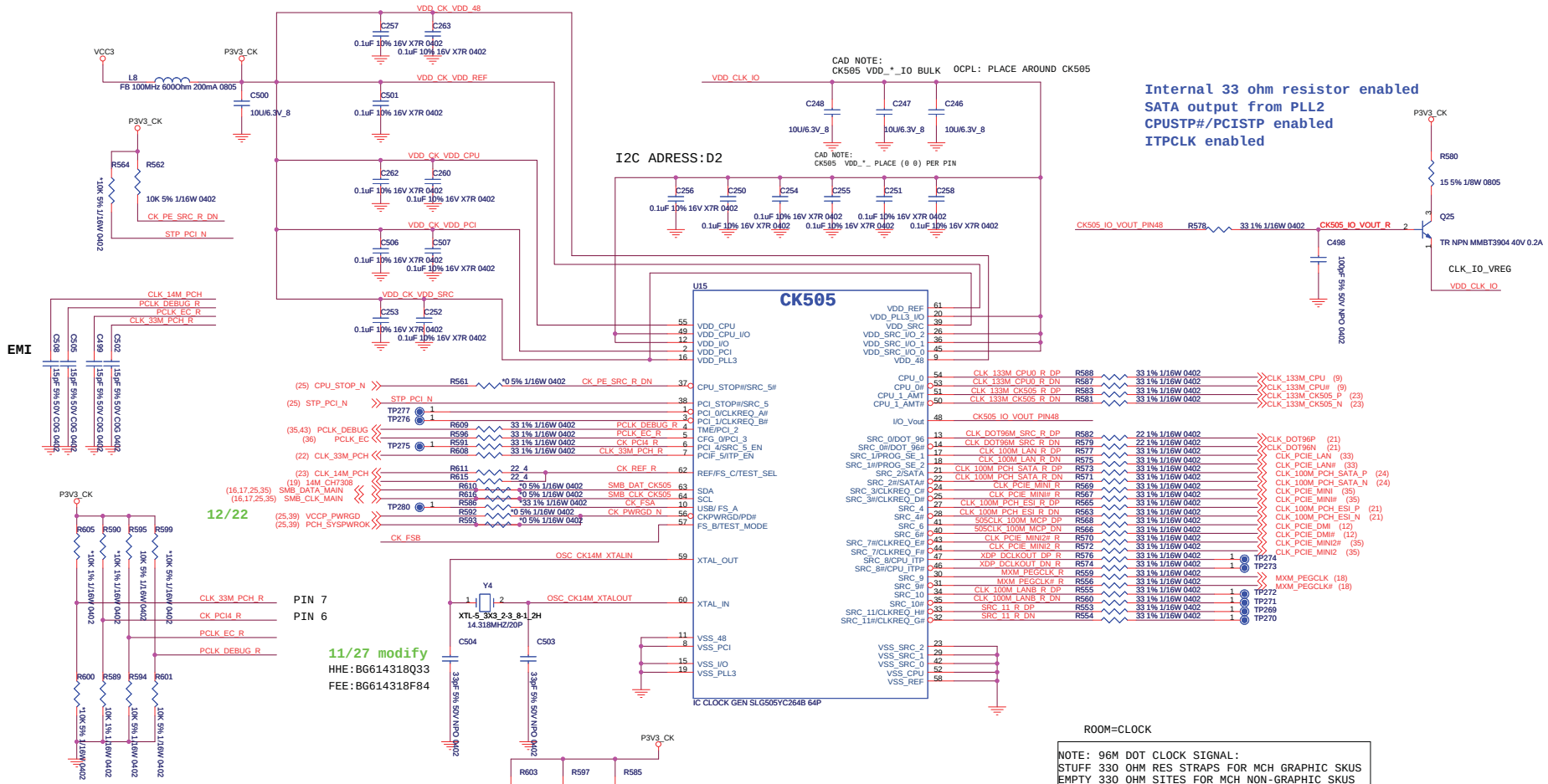
Title: MODIFY CHANGE LIST

Size	Document Number	Rev
C	EL5	A02



		High	Low
PIN 1	PCI_0/CLKREQ_A#		
PIN 3	PCI_0/CLKREQ_B#		
PIN 6	PCI_4/SRC_5_EN	SRC5+/- 37,38	CPU_STOP#
PIN 7	PCI_4/SRC_5_EN	SRC8+/- 46,47	CPU_ITP

PIN 5	PIN 4	PLL	PLL1	SSC	PLL3	SSC
Low	Low	0	CPU/SRC/PCI	Down	LCDCLK	Down
Low	High	0	CPU/SRC/PCI	Down	LCDCLK	Down
Mid	Low	1	CPU	Down	SRC/PCI	Down
Mid	High	1	CPU	Down	SRC/PCI	Down
High	Low	2	CPU	Center	SRC/PCI	Down
High	High	3	CPU	Center	SRC/PCI	Down

PIN 17/18 SRC1 SSC

SEL2 SEL1 SEL0 Frequence select

FSC	FSB	FSA	CPU	SRC	PCI	
0	0	0	266	100	33	
0	0	1	133	100	33	Default
0	1	0	200	100	33	
0	1	1	166	100	33	
1	0	0	333	100	33	
1	0	1	100	100	33	
1	1	0	400	100	33	
1	1	1	Reserved			

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Title: CK505_B CLOCK GENERATOR
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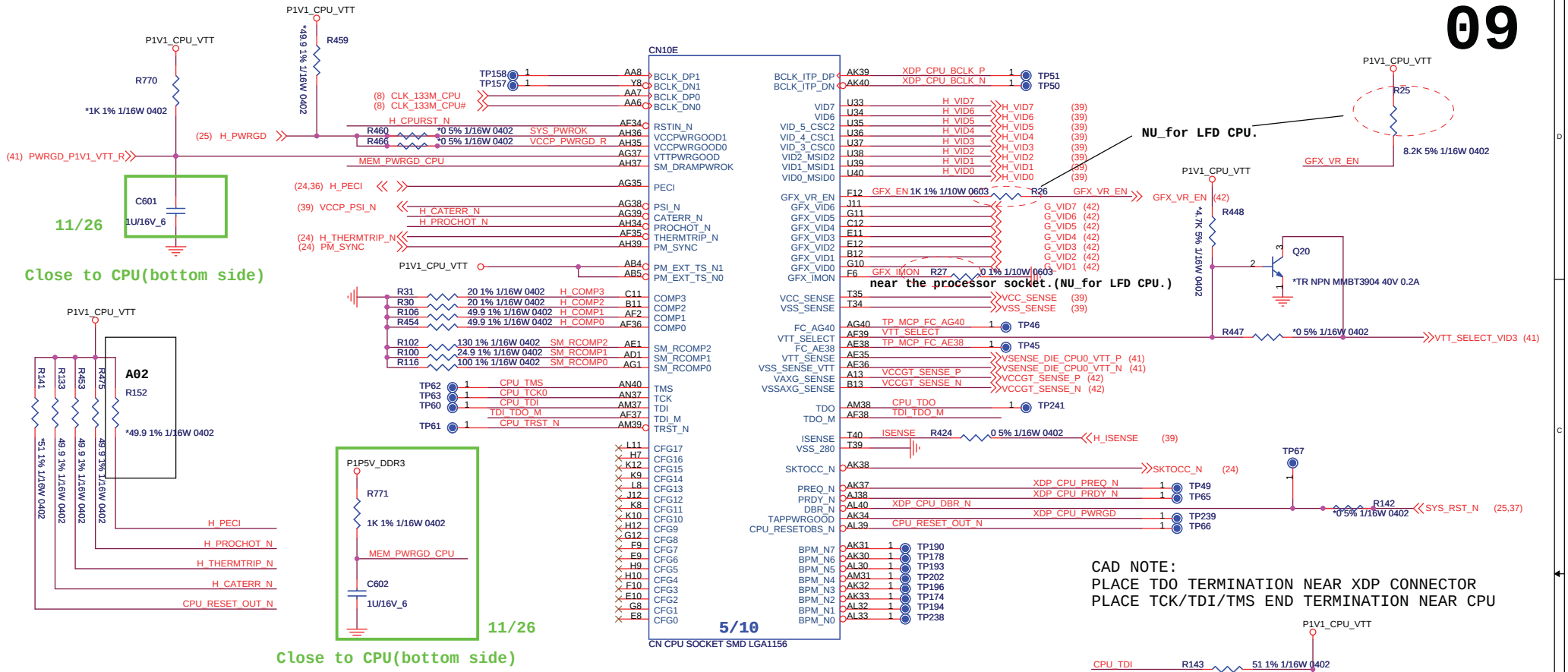
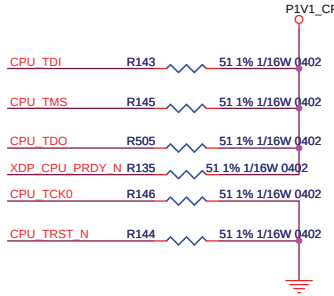


CAD NOTE:
PLACE TDO TERMINATION NEAR XDP CONNECTOR
PLACE TCK/TDI/TMS END TERMINATION NEAR CPU

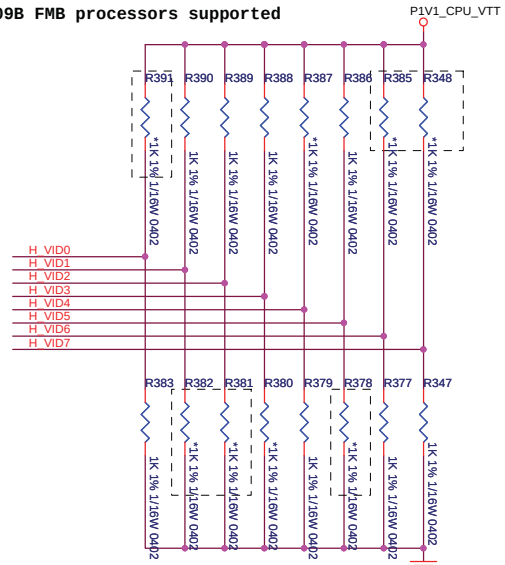


CPU HAS INTEGRATED TCK/TMS/TDI TERMINATION.

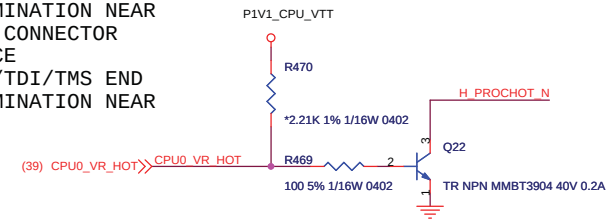
CFG	H	L	Notes
0			H:1x16, L:2x8
1	RSVD		
2	RSVD		
3	NORM	RSVD	LANE REVERSAL
4	DISABLE	ENABLE	DP PRESENCE
5	RSVD		
6	RSVD		

CFG 0-6 all internal PULL-UP

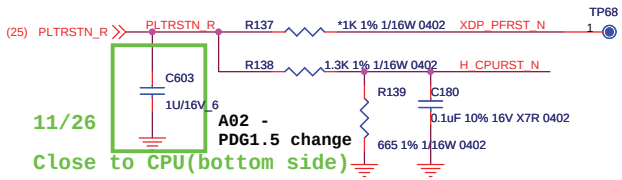
VID[7:0] : 00101110 =>1.325V@VCC,Max
2009B FMB processors supported



CAD NOTE:
PLACE TDO TERMINATION NEAR XDP CONNECTOR
PLACE TCK/TDI/TMS END TERMINATION NEAR CPU



Need to be placed close to processor to minimize ESD risk



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Title	MCP - CLK,CTRL,MISC,DEBUG		
Size Custom	Document Number EL5		Rev A02
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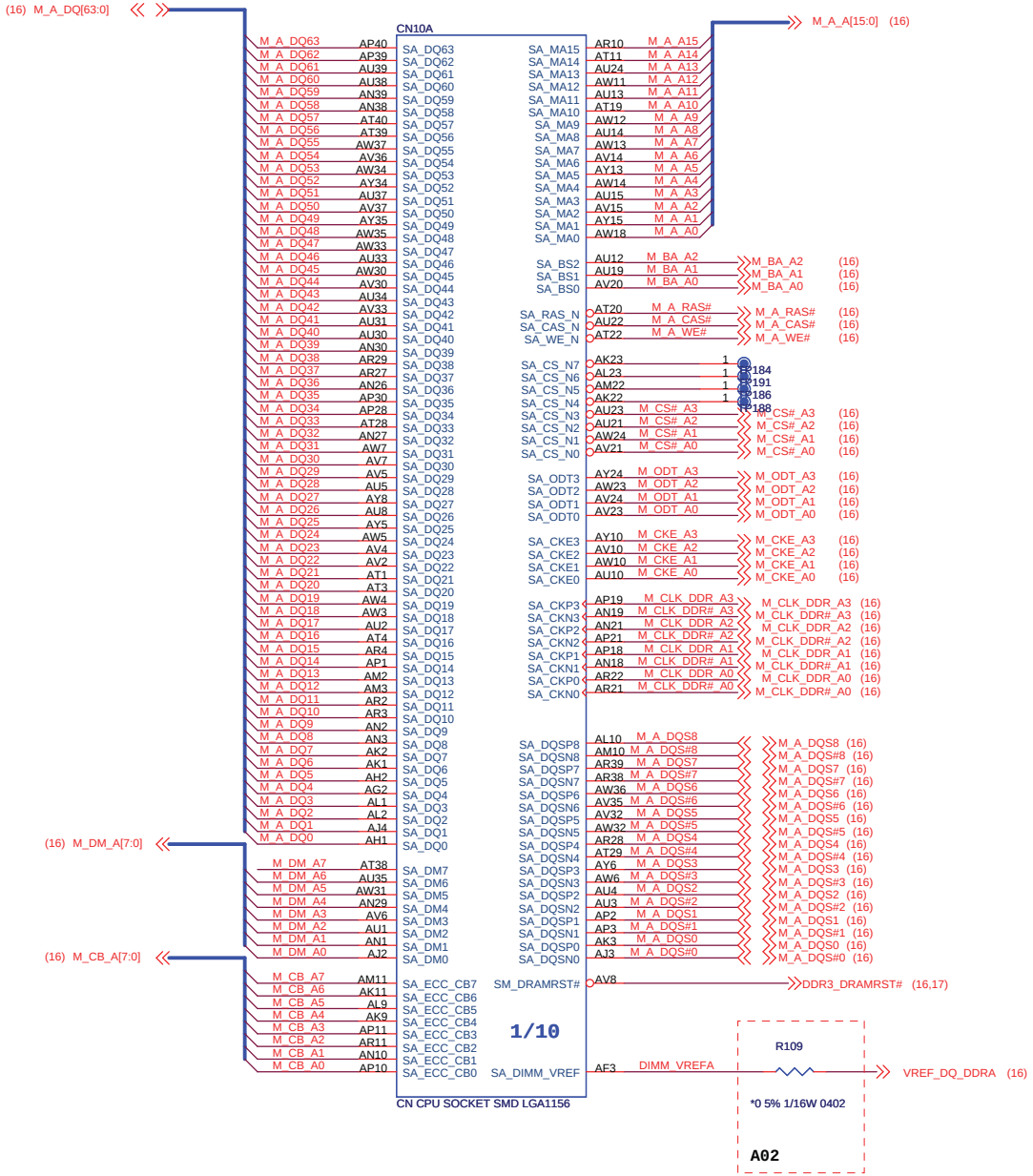

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Title	MCP - DDR3 CHANNEL A	
Size Custom	Document Number EL5	Rev A02
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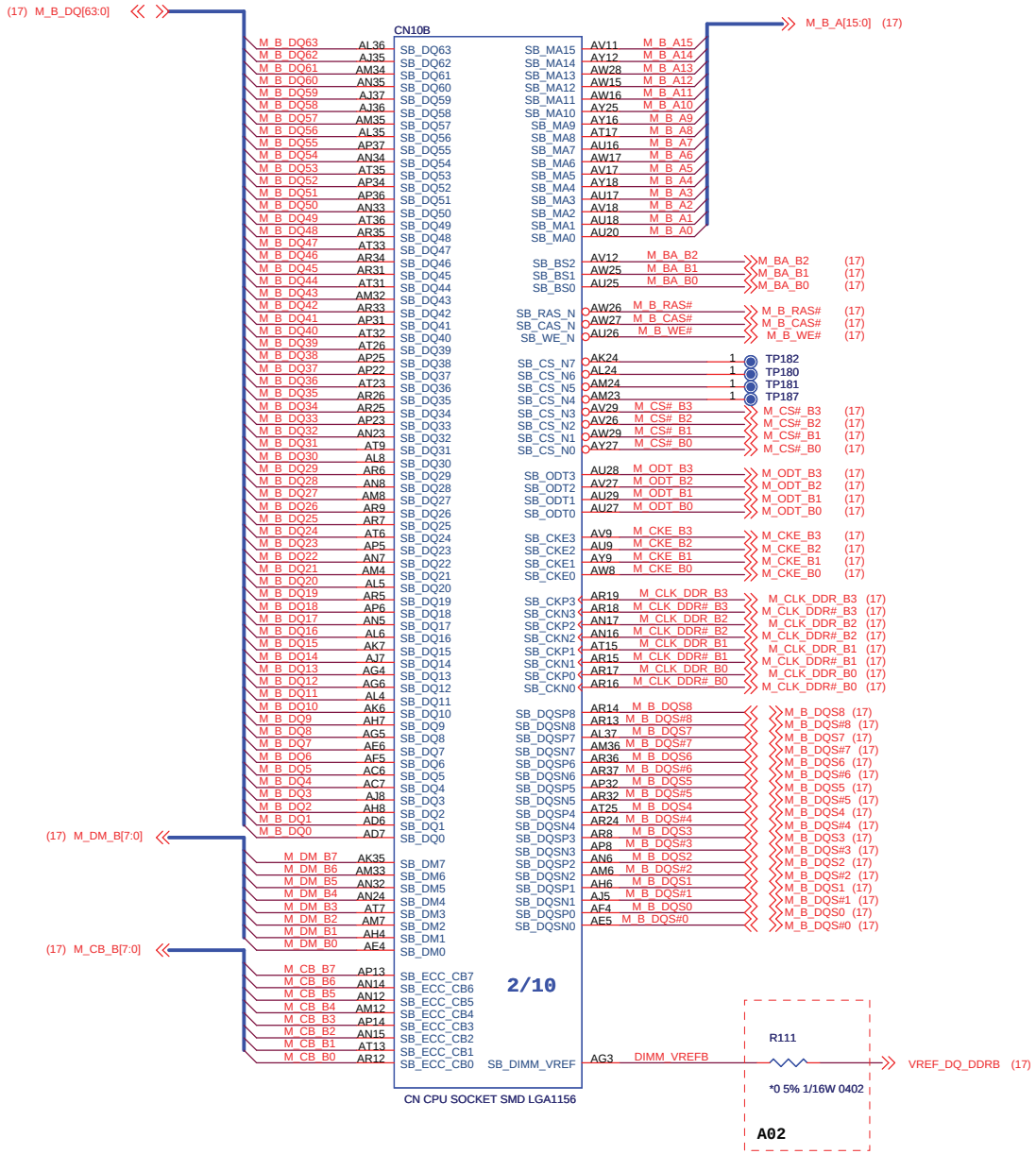

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Title	MCP - DDR3 CHANNEL B		
Size Custom	Document Number EL5		Rev A02
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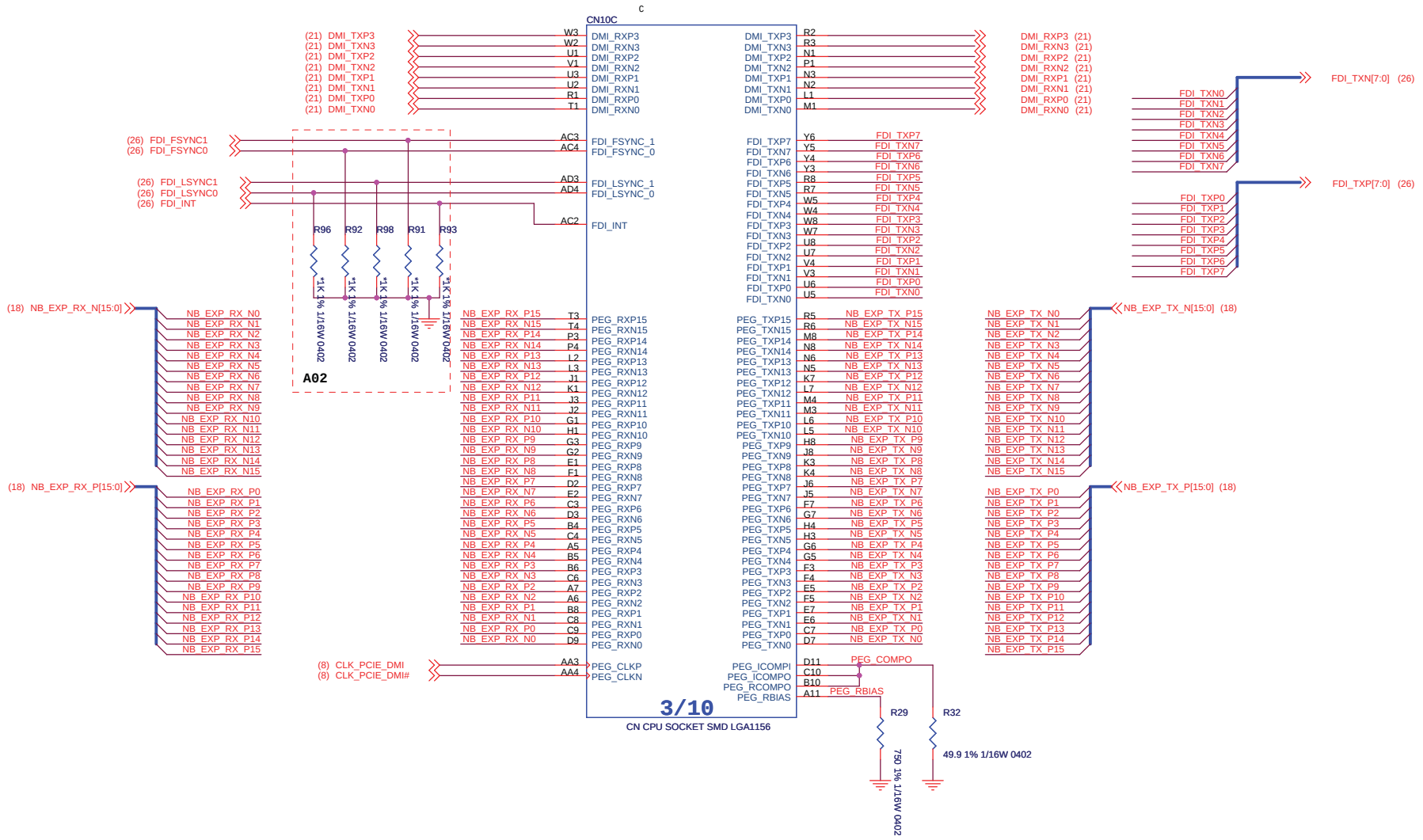

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Title	MCP - PCIE, DMI	
Size Custom	Document Number EL5	Rev A02
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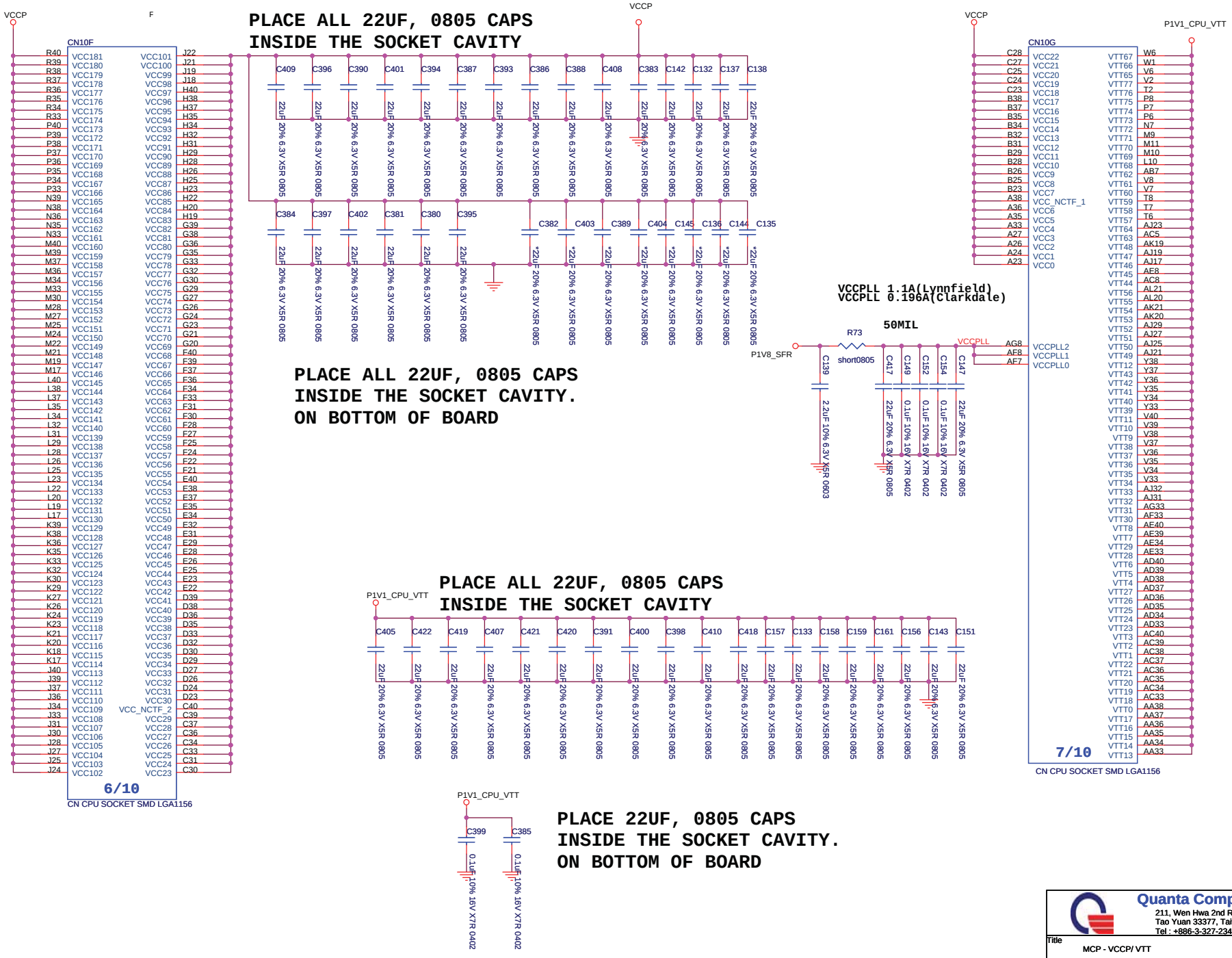

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Title	MCP - VCCP/ VTT	
Size Custom	Document Number EL5	Rev A02
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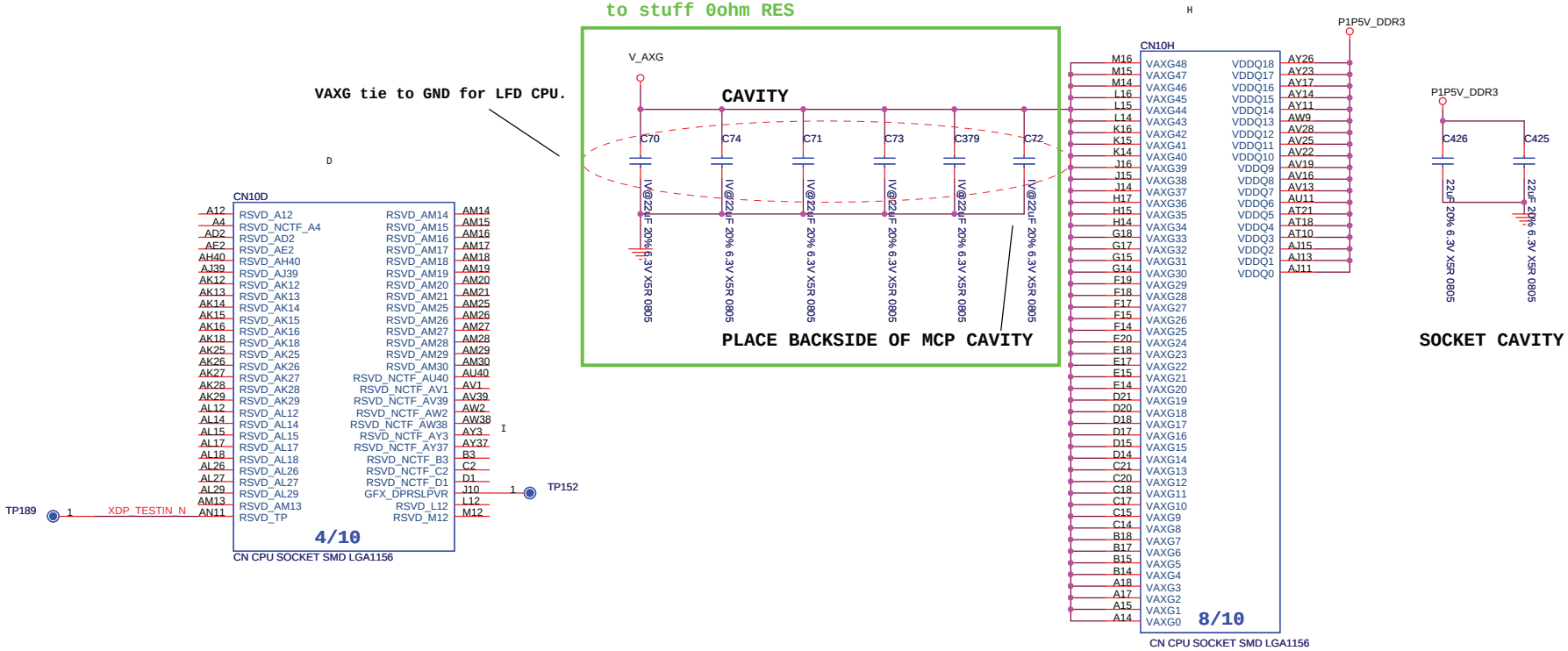
BOM note:
EV@C70、C71、C72、C73、C74、C379 need to stuff 0ohm RES

VAXG tie to GND for LFD CPU.



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Title	MCP - V_AXG/ P1P5V_DDR3		
Size Custom	Document Number EL5		Rev A02
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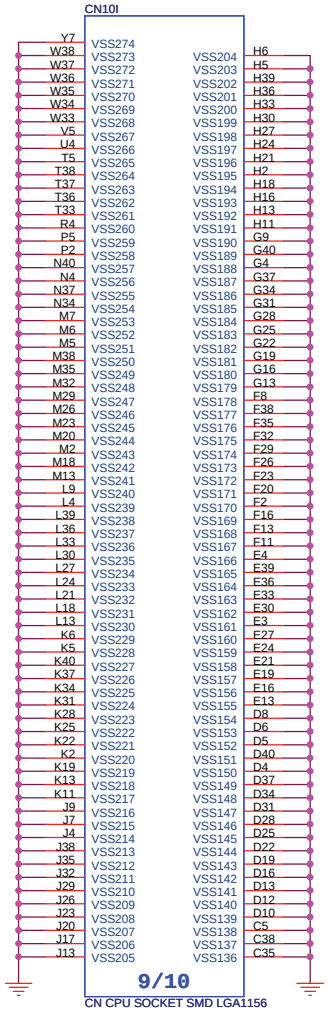
J



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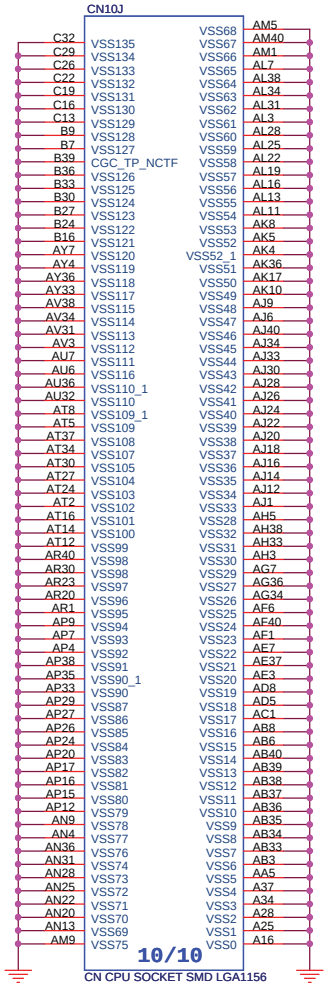

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Title	MCP - GND	
Size Custom	Document Number EL5	Rev A02
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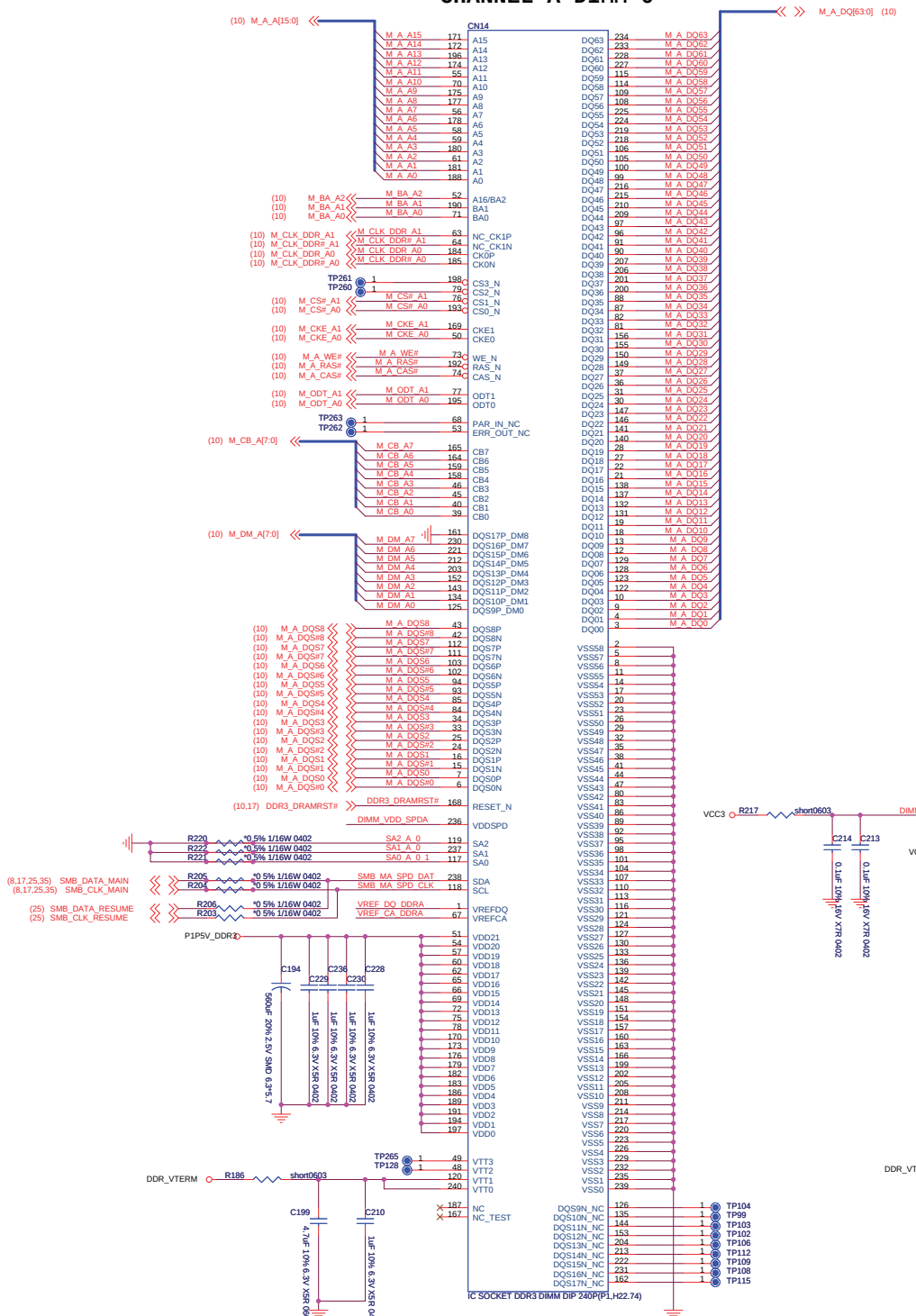
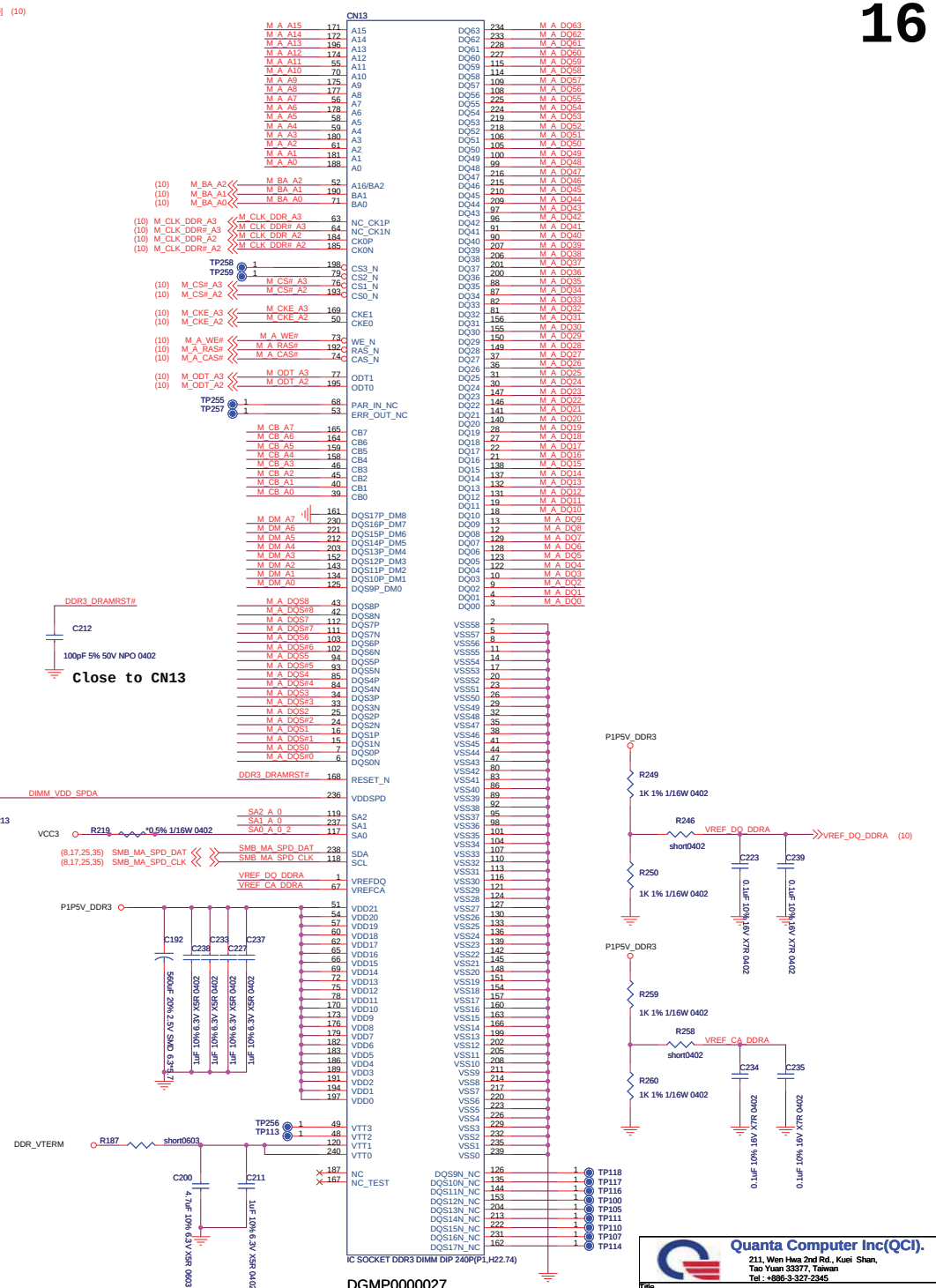
CHANNEL A DIMM 0



CHANNEL A DIMM 1



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Title		
DDRIII CHANNEL A		
Size C	Document Number EL5	Rev A02
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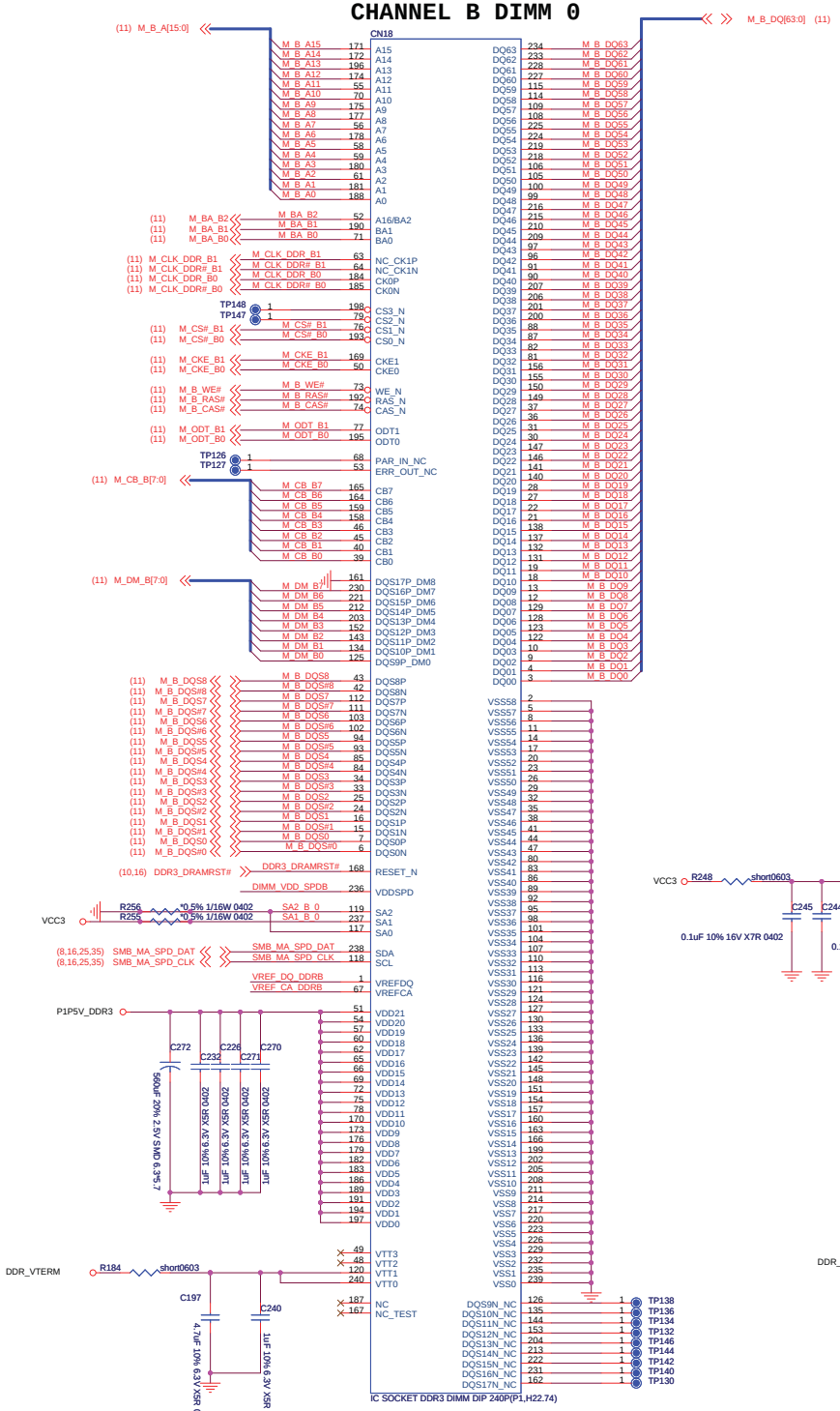
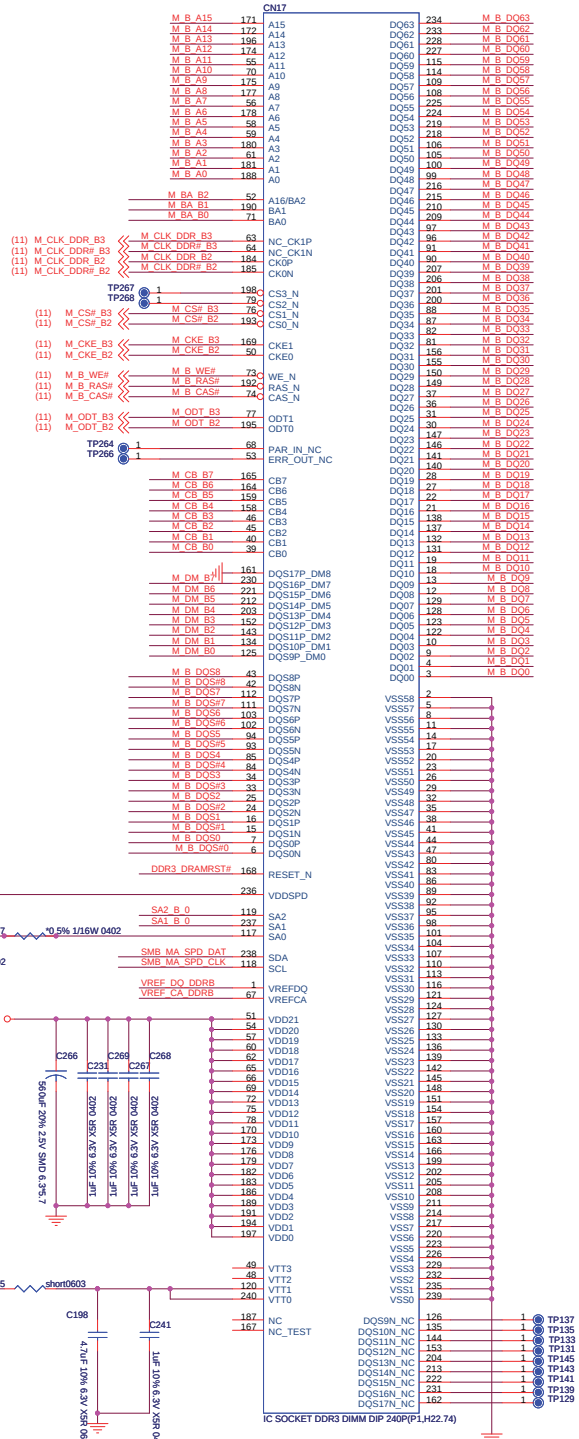
CHANNEL B DIMM 0

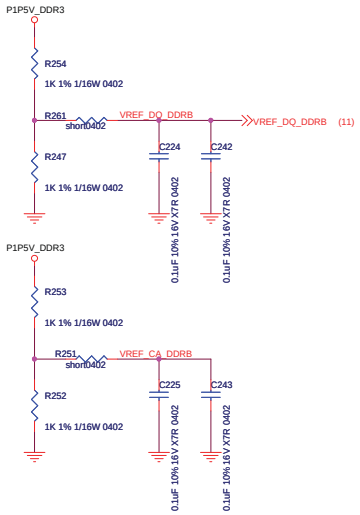


DGMP0000028

CHANNEL B DIMM 1



DGMP0000027



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Title	DDRIII CHANNEL B	
Size C	Document Number EL5	Rev A02
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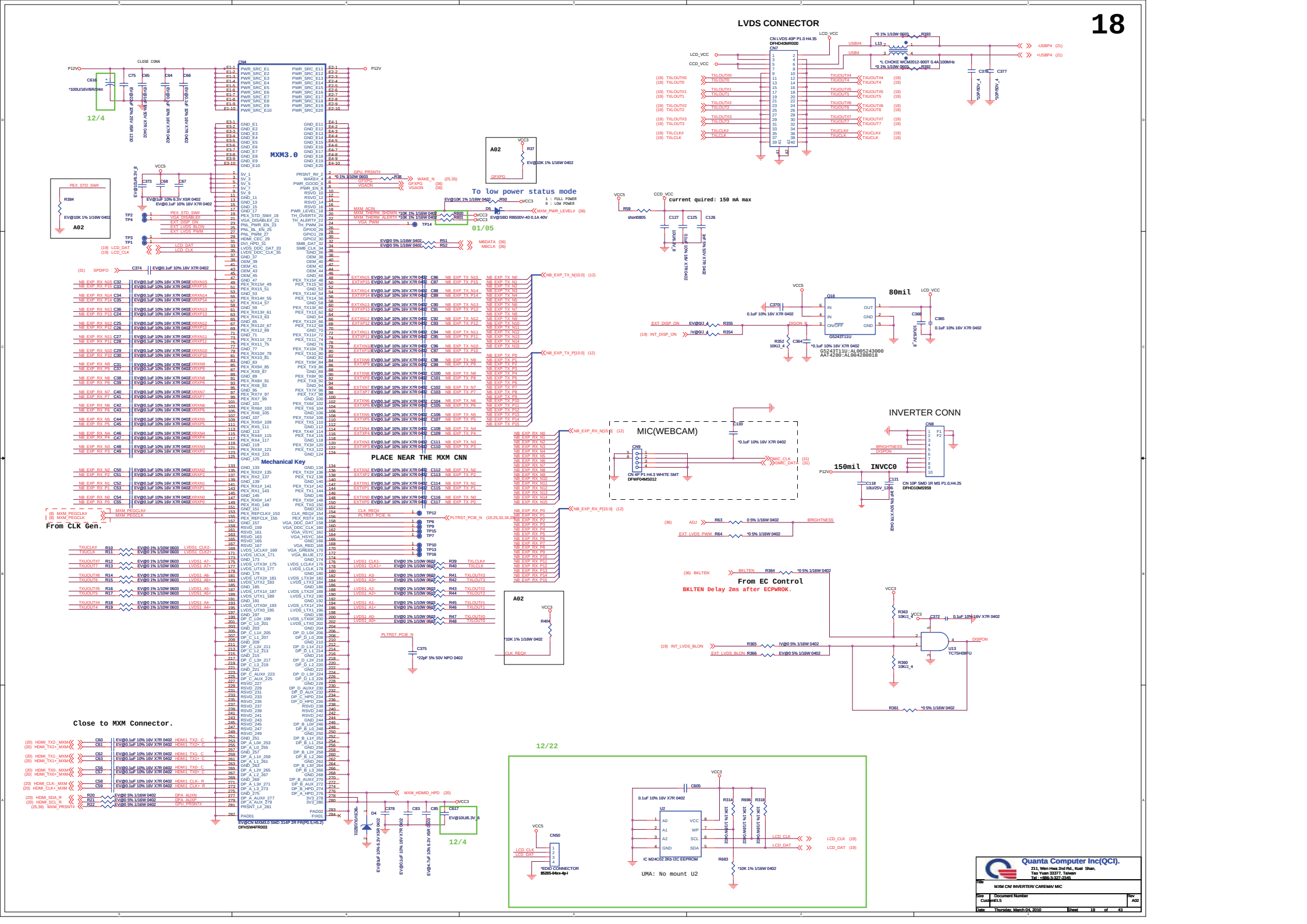
LVDS CONNECTOR
CN LVDS 40P P1.0 H4.35
DFHD40MR000
CN7
MXM3.0
CN4
12/4
01/05
To low power status mode
current quired: 150 mA max
80mil
G5243T11U
INVERTER CONN
CN8
150mil
INVCC0
CN 10P SMD 1R MS P1.0,H4.25
DFHD10MS959
MIC(WEBCAM)
CN 4P P1 H4.3 WHITE SMT
DFWF04MS012
PLACE NEAR THE MXM CNN
Mechanical Key
From CLK Gen.
From EC Control
BKLTEN Delay 2ms after ECPWROK.
Close to MXM Connector.
12/22
CN50
*EDID CONNECTOR
85205-04xx-4p-l
IC M24C02 2Kb I2C EEPROM
UMA: No mount U2
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MXM CN/ INVERTER/ CAREMA/ MIC
Size: CustomEL5
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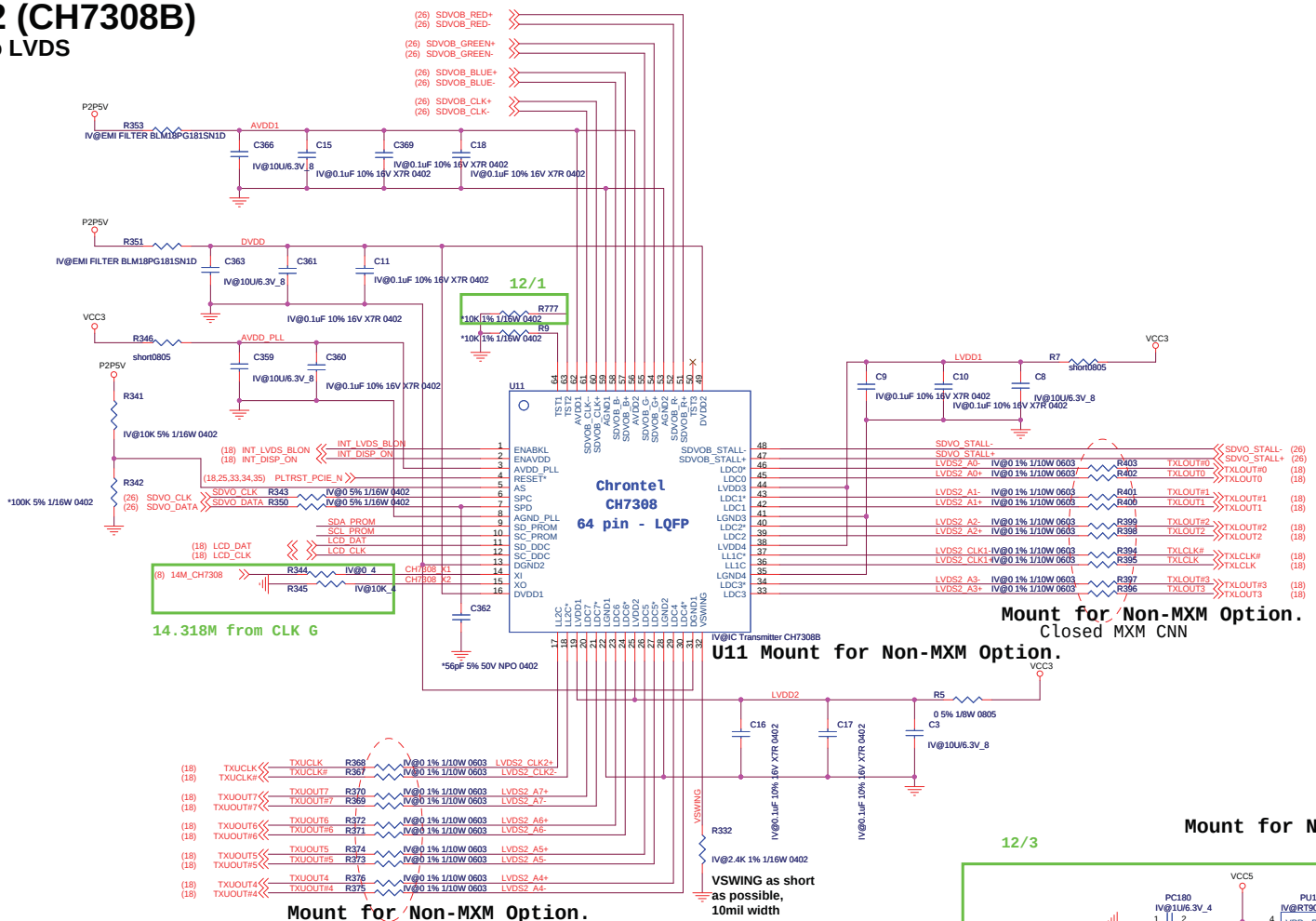
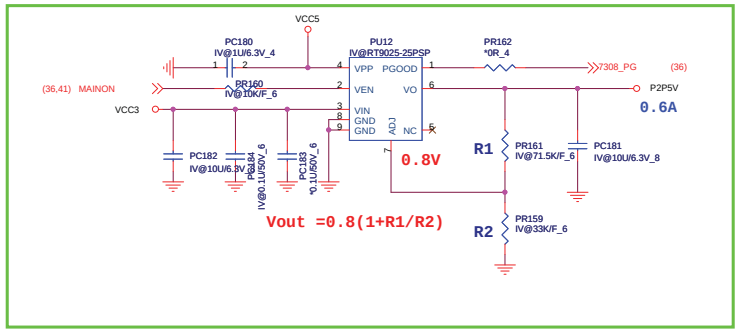
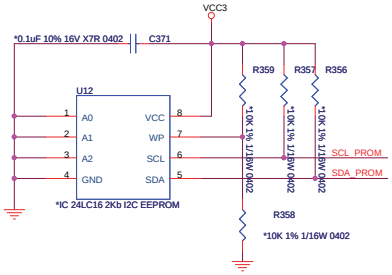
LVDS2 (CH7308B)

SDVOB to LVDS







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Title	LVDS TRANSMITTER-CH7308	
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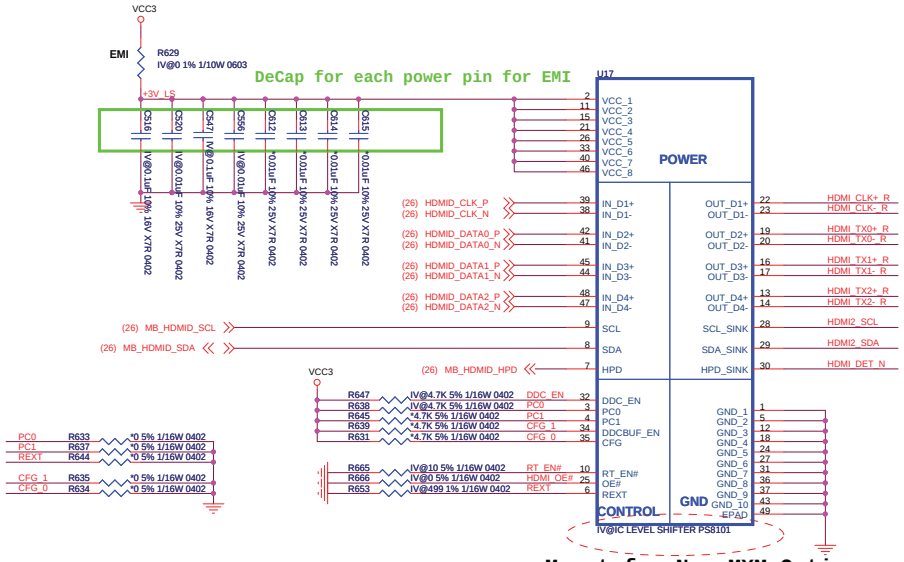
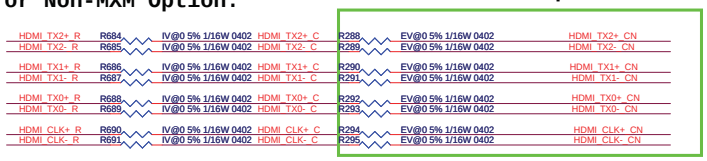


Mount for Non-MXM Option.

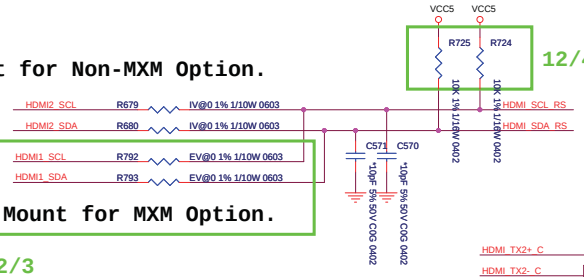
EQUALIZATION SETTING
PC1:PC0=0:0 8dB
PC1:PC0=0:1 4dB Recommanded
PC1:PC0=1:0 12dB
PC1:PC0=1:1 0dB

Mount for Non-MXM Option.

Mount for MXM Option.

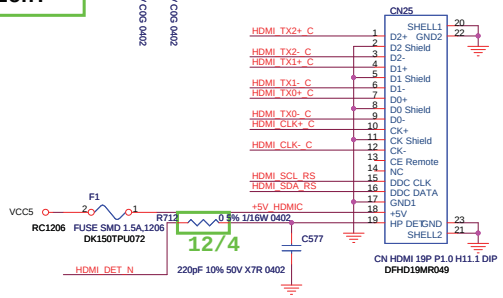


Mount for Non-MXM Option.



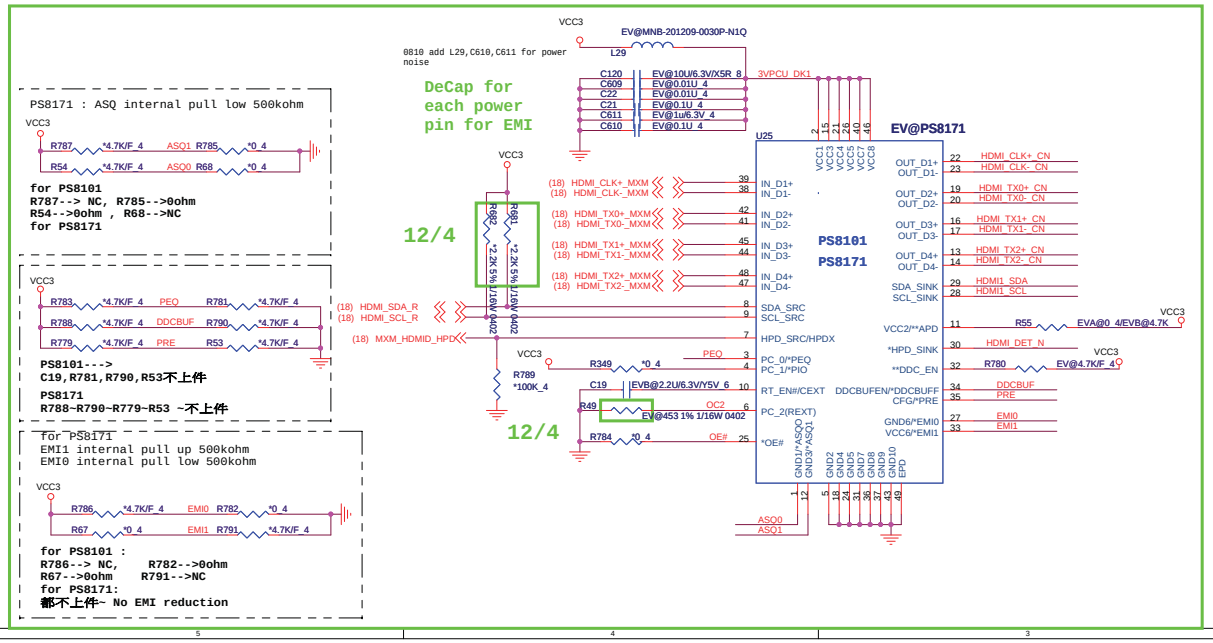
Mount for MXM Option.

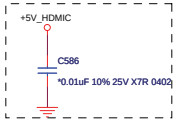
12/3



EVA@: PS8101
EVB@: PS8171
EV@MXM
IV@UMA

12/3





for EMI request

PS8171 EMI		
EMI0	EMI1	EMI reduction and filter setting
L	L	
L	H	※ no EMI reduction
H	L	
MID	MID	

PS8171 HPDX		
PIN4	LEVEL	HPDX Output
PIO	L	※ HPD_Sink = HPD
	H	HPD=HPD_SINK#

PS8171 APD (ASQ internal pull low 500kohm)		
PIN11	LEVEL	Description
APD	HIGH	Automatic power down enable
	MID	
	LOW	Automatic power down disable

PS8171 ASQ (ASQ internal pull low 500kohm)		
PIN1 PIN12	LEVEL	Automatic Squelch
ASQ[1,0]	HL	No automatic squelch
	LL	※ Level=100mVpp,default timer
	LH	Level=150mVpp,default timer
	HH	Level=200mVpp,default timer
	ML	Level=120mVpp,extended timer
	MH	Level=100mVpp,extended timer
	LM	Level=80mVpp,extended timer
	HM	Reserved
	MM	Reserved

PRE internal pull low 500kohm

PS8171 DDCBUF (DDCBUF internal pull low 500kohm)		
PIN34	LEVEL	Description
DDCBUF	HIGH	Active DDC buffer enable;Setting 1
	MID	Active DDC buffer enable;Setting 2
	LOW	※ No DDC active buffer,passive DDC level shifting

PS8171 EQ		
PIN3	LEVEL	EQ
PEQ	HIGH	7dB
	MID	※ 2dB
	LOW	4dB

PS8171 SWING		
PIN35	LEVEL	dB
PRE	HIGH	1.2dB
	MID	2dB
	LOW	※ 0dB

PC1	PC0	EQUALIZATION
0	0	8dB
0	1	※ 4dB
1	0	12dB
1	1	0dB

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Title: HDMI, LEVEL SHIFTER-PS8101

Size: C | Document Number: EL5 | Rev: A02

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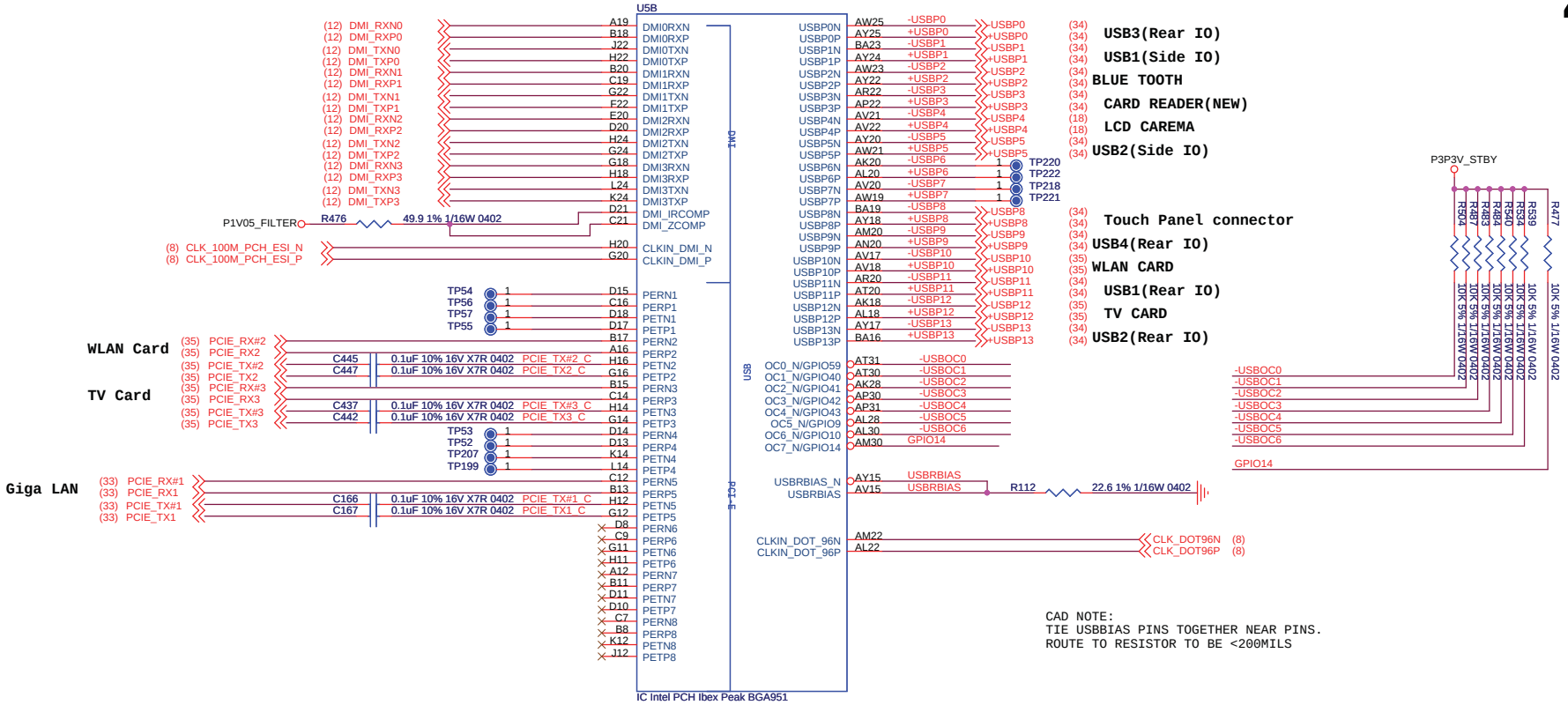

CAD NOTE:
TIE USBBIAS PINS TOGETHER NEAR PINS.
ROUTE TO RESISTOR TO BE <200MILS

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Title	PCH-DMI, PCI-E, USB		
Size Custom	Document Number EL5		Rev A02
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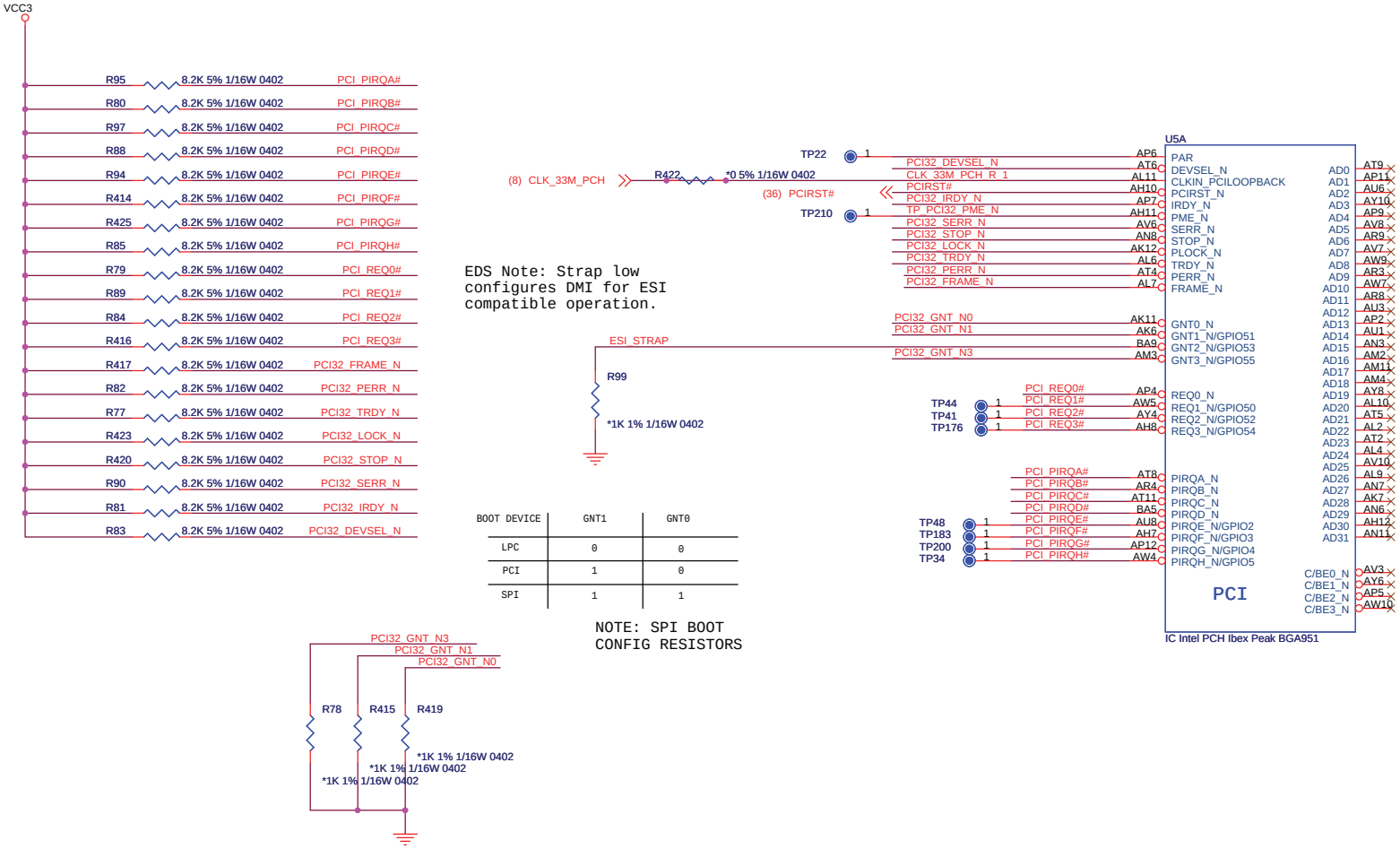

BOOT DEVICE	GNT1	GNT0
LPC	0	0
PCI	1	0
SPI	1	1

NOTE: SPI BOOT CONFIG RESISTORS

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Title: PCH-PCI

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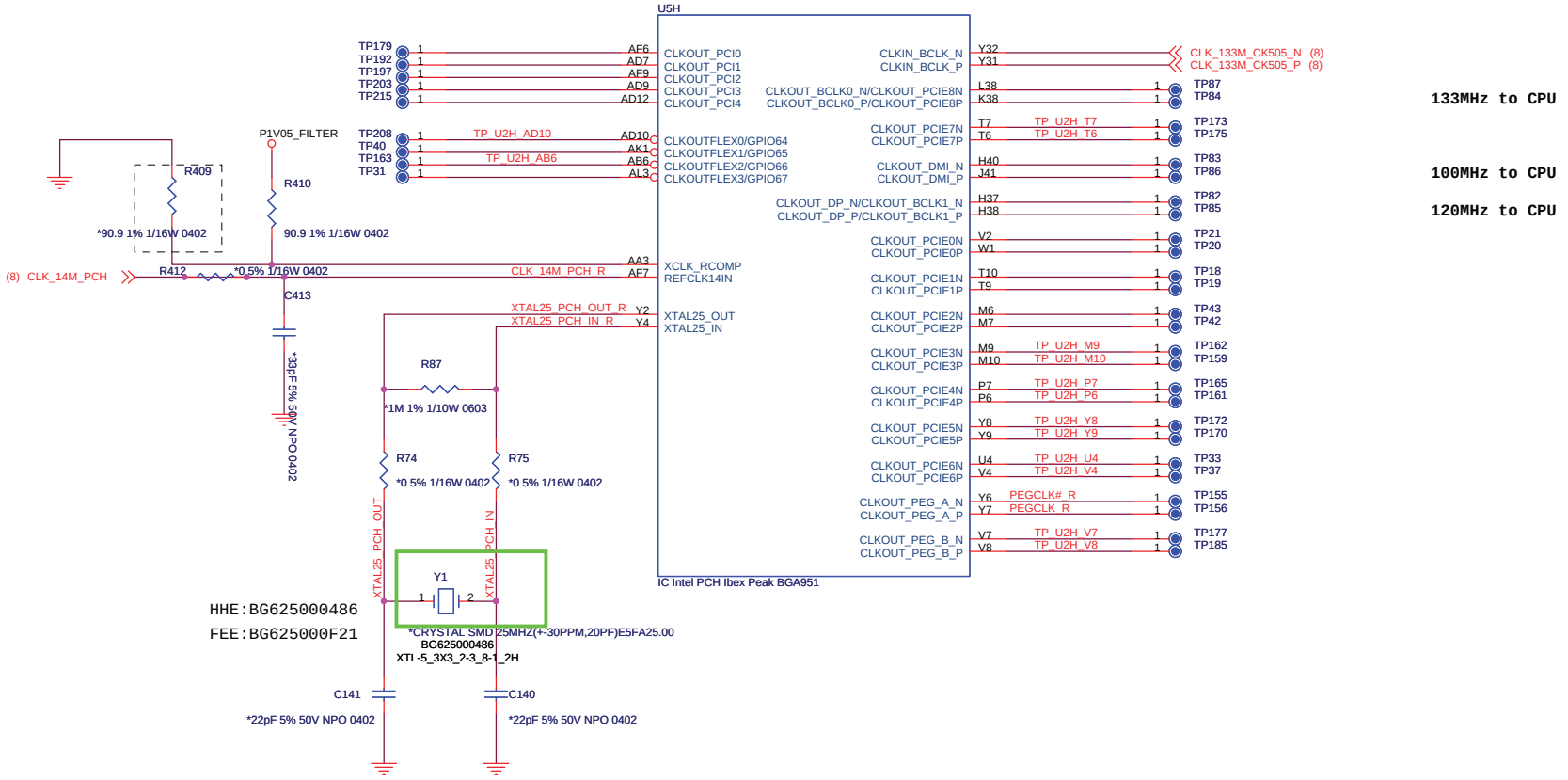

133MHz to CPU

100MHz to CPU

120MHz to CPU

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Title: PCH-CLOCK DISTRIBUTION

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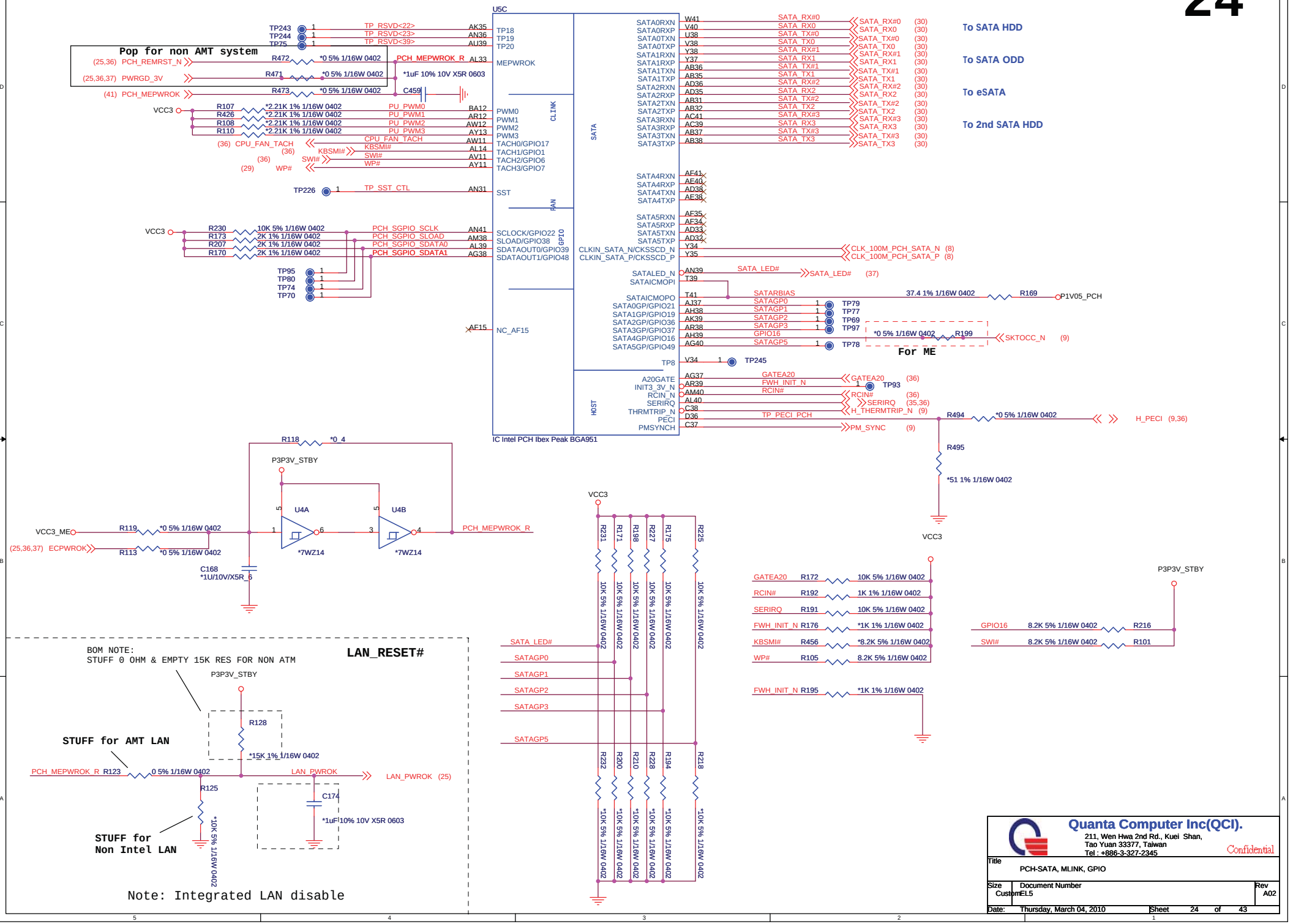

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Title	PCH-SATA, MLINK, GPIO	
Size Custom	Document Number EL5	Rev A02
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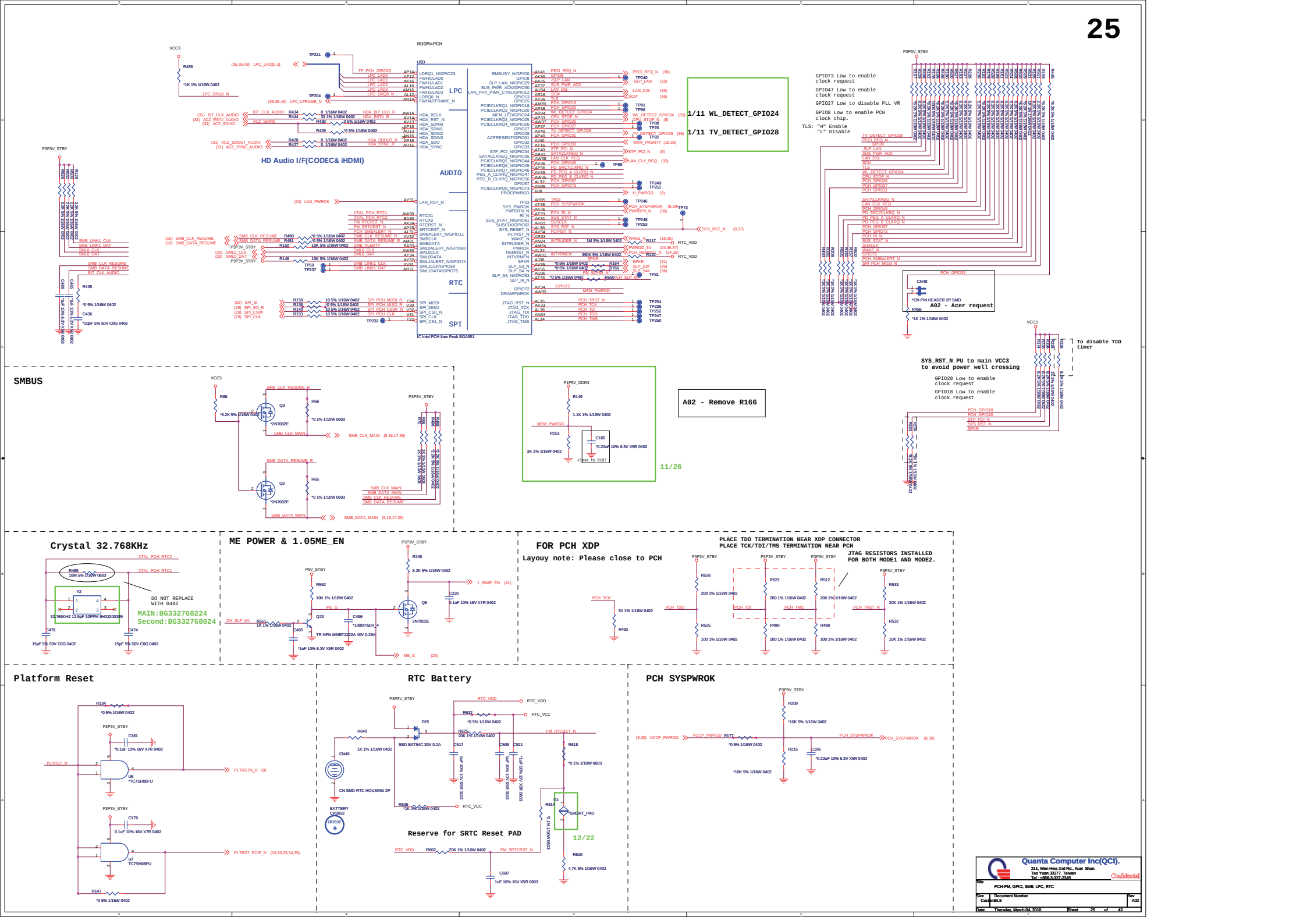
ROOM=PCH
HD Audio I/F(CODEC& iHDMI)
LPC
AUDIO
RTC
SPI
1/11 WL_DETECT_GPIO24
1/11 TV_DETECT_GPIO28
GPIO73 Low to enable clock request
GPIO47 Low to enable clock request
GPIO27 Low to disable PLL VR
GPIO8 Low to enable PCH clock chip.
TLS: "H" Enable "L" Disable
A02 - Acer request
SYS_RST_N PU to main VCC3 to avoid power well crossing
GPIO20 Low to enable clock request
GPIO18 Low to enable clock request
To disable TCO timer
SMBUS
A02 - Remove R166
11/26
Crystal 32.768KHz
DO NOT REPLACE WITH 0402
MAIN:BG332768224
Second:BG332768024
ME POWER & 1.05ME_EN
FOR PCH XDP
Layouy note: Please close to PCH
PLACE TDO TERMINATION NEAR XDP CONNECTOR
PLACE TCK/TDI/TMS TERMINATION NEAR PCH
JTAG RESISTORS INSTALLED FOR BOTH MODE1 AND MODE2.
Platform Reset
RTC Battery
Reserve for SRTC Reset PAD
12/22
PCH SYSPWROK
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PCH-PM, GPIO, SMB, LPC, RTC
Size: Custom
Document Number: EL5
Rev: A02
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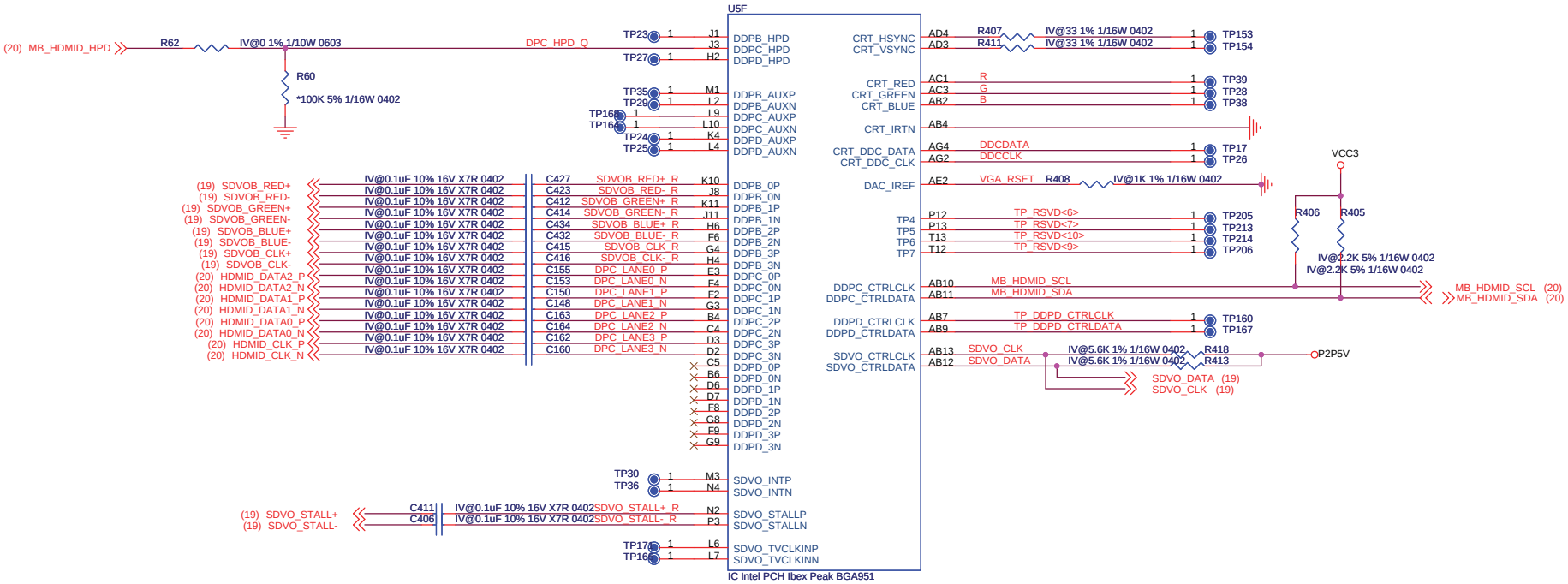

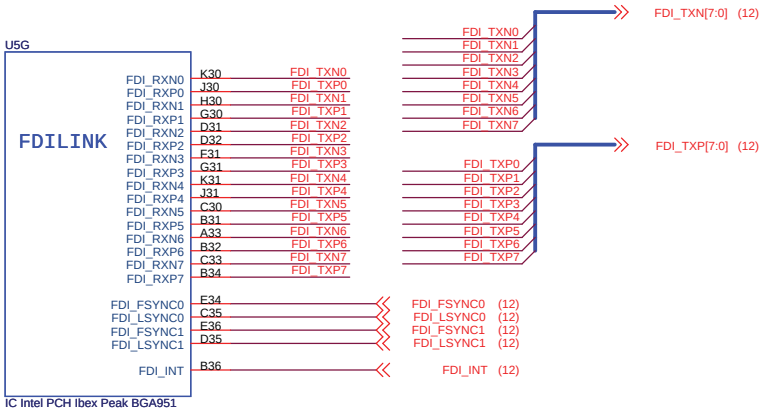

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Title	PCH-DISPLAY , FDILINK
Size Custom	Document Number EL5
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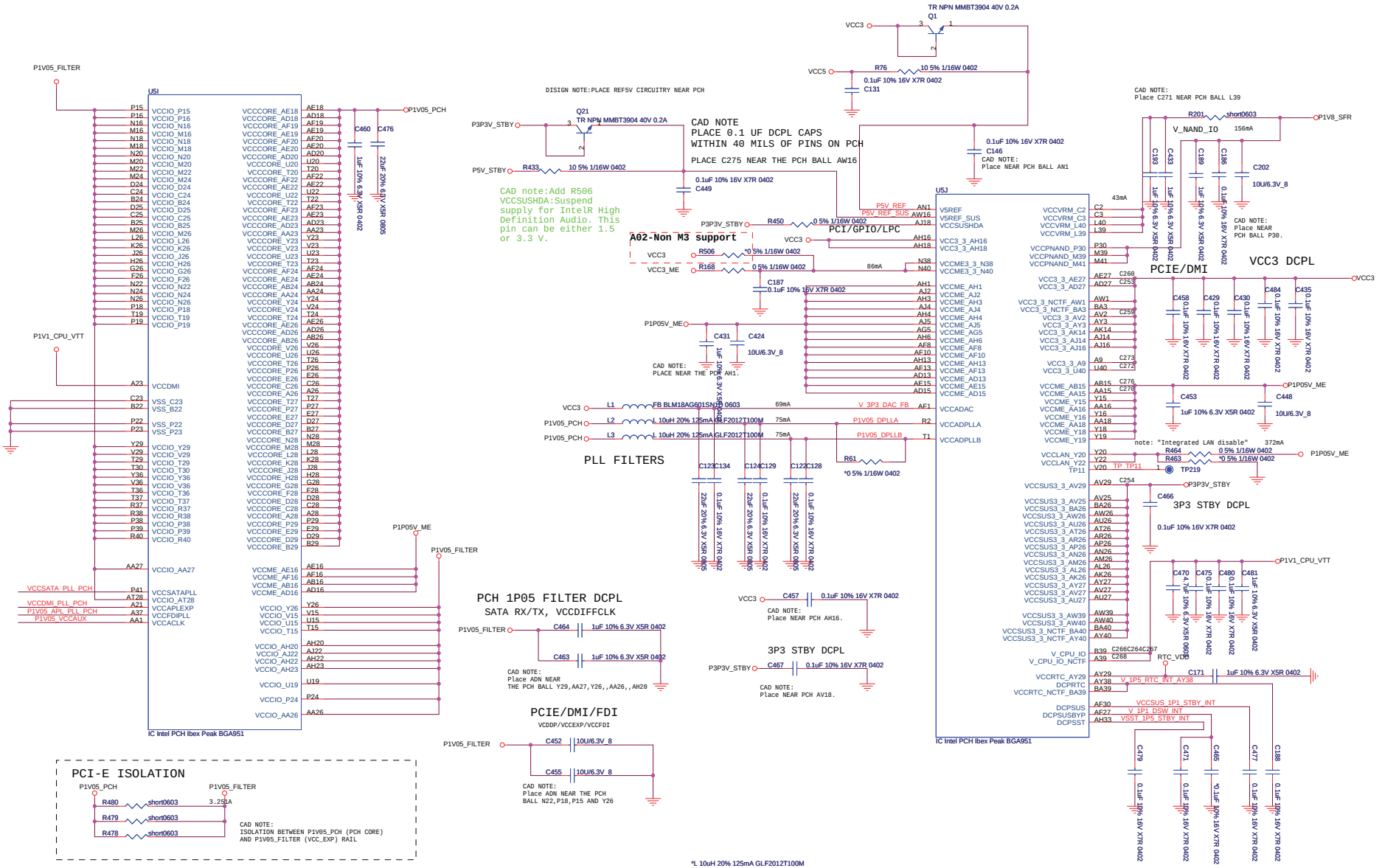

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Title	PCH-POWER	
Size C	Document Number EL5	Rev A02
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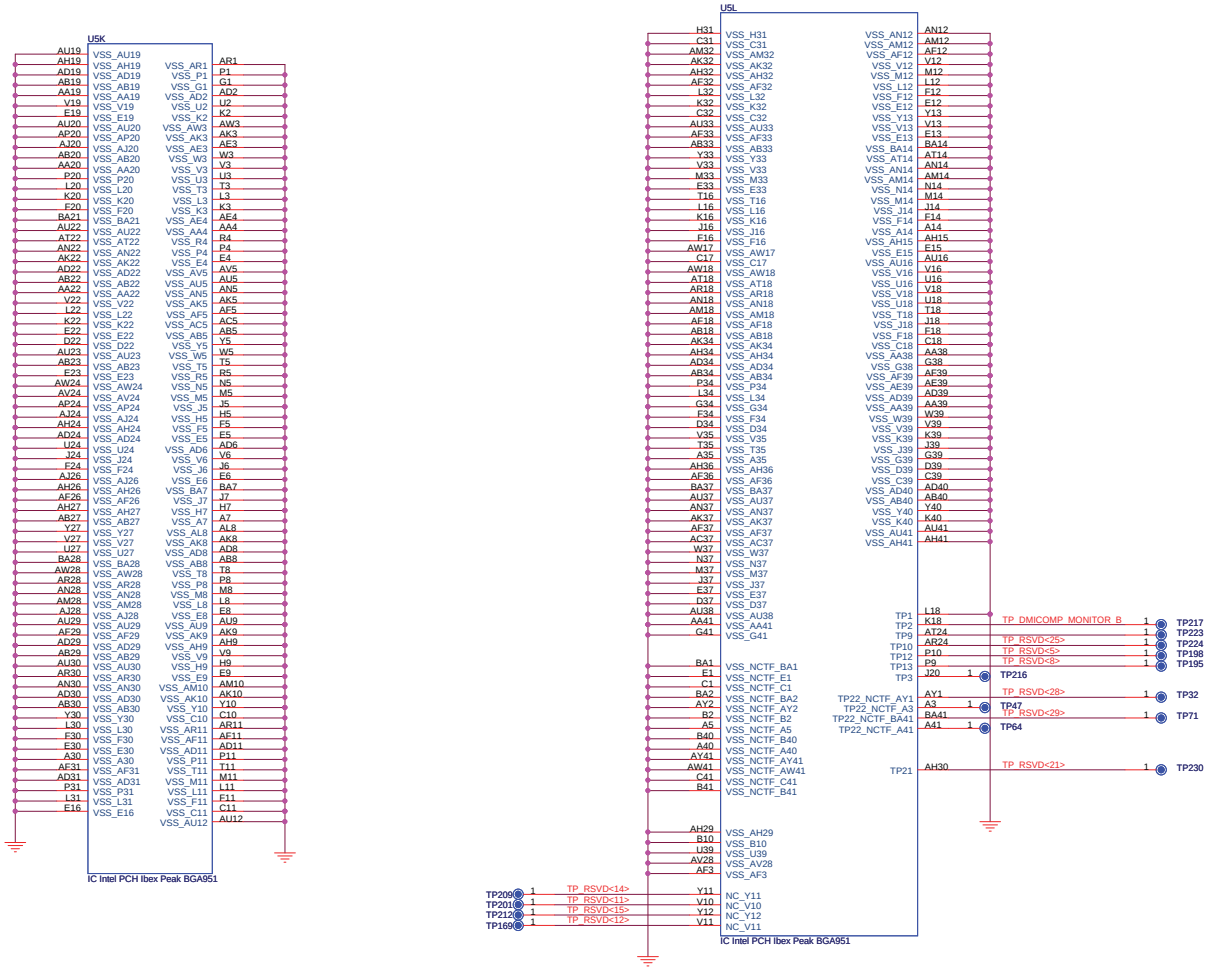

PCH - GND

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Title		
PCH-GND		
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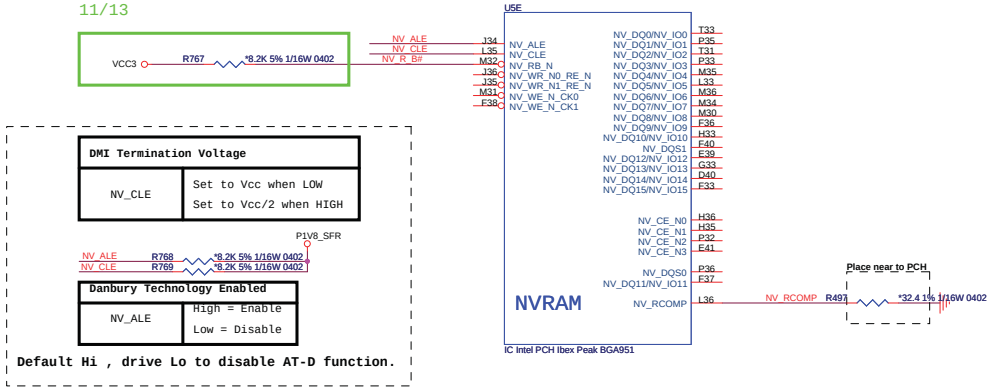
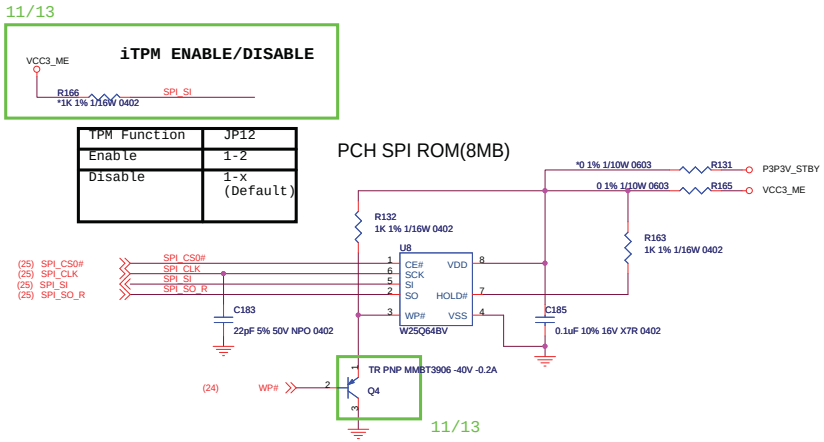
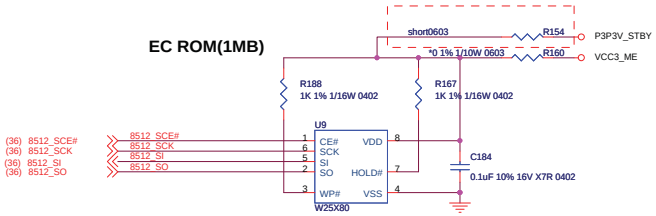
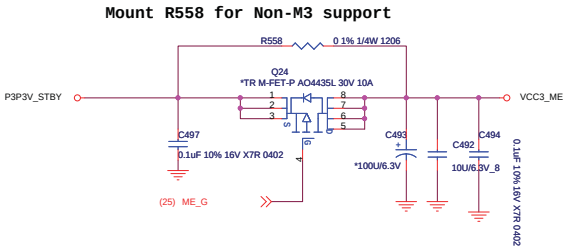


Note: For NV_ALE, Intel Anti-Theft Technology is enabled when sampled high . pulling the signal low disable Intel Anti-Theft Technology

Note: NV_CLE signal should not be pulled low during the time the strap is sampled







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Title	PCH-NV RAM (ONFI)/FLASH	
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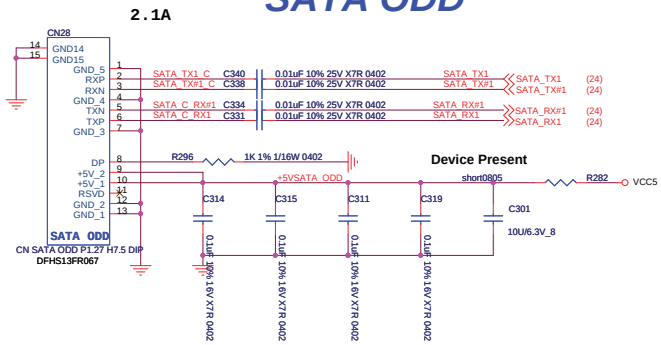
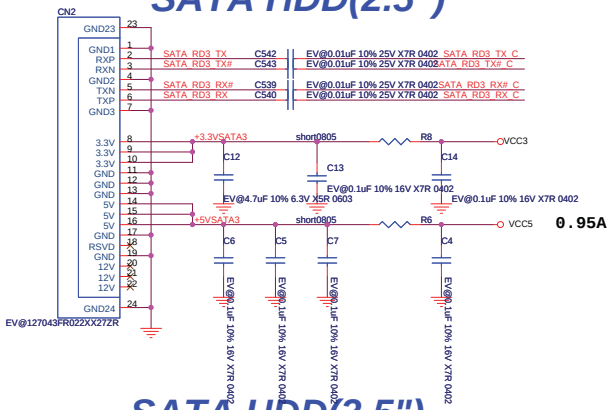
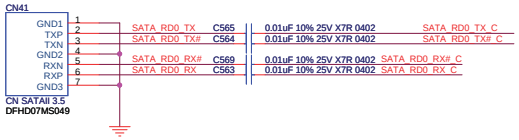
SATA ODD



SATA HDD(2.5")

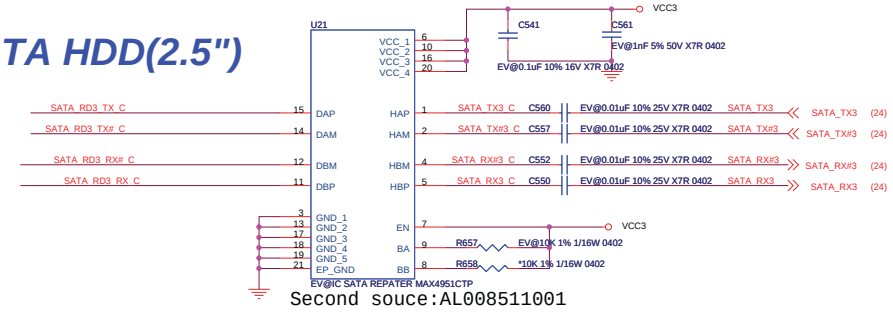


SATA HDD(3.5")



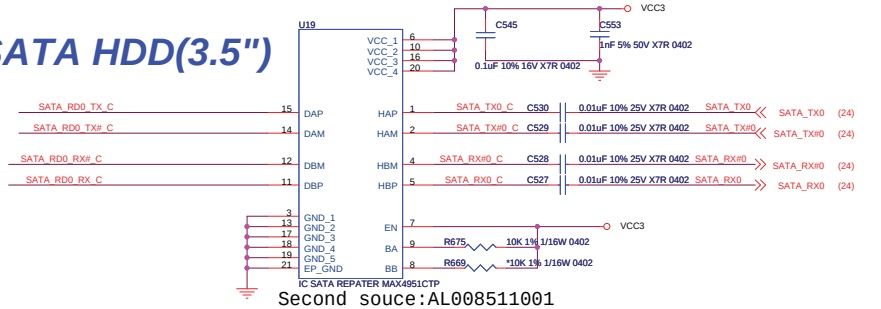
ESATA CONN

SATA HDD(2.5")



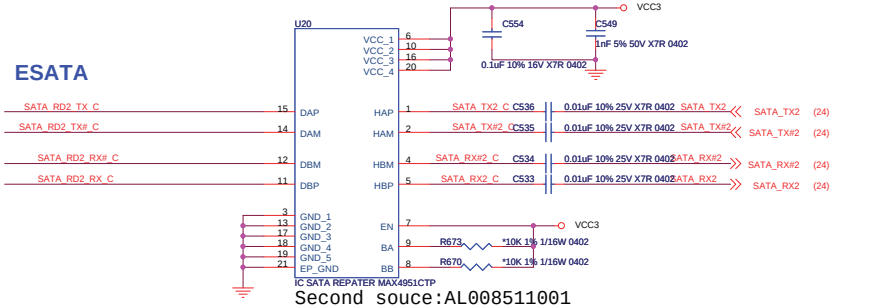
Second souce:AL008511001

SATA HDD(3.5")



Second souce:AL008511001

ESATA



Second souce:AL008511001

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Title		
ESATA,ODD,2.5/3.5HDD		
Size C	Document Number EL5	Rev A02
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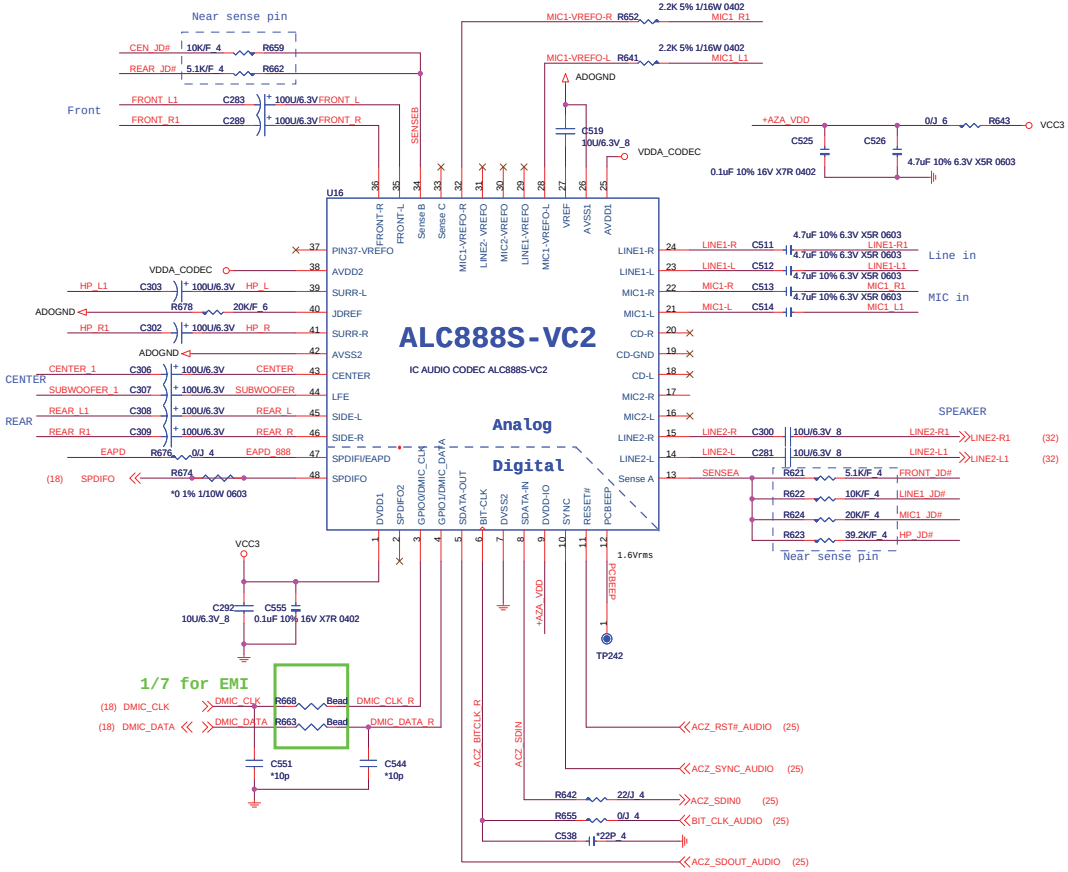
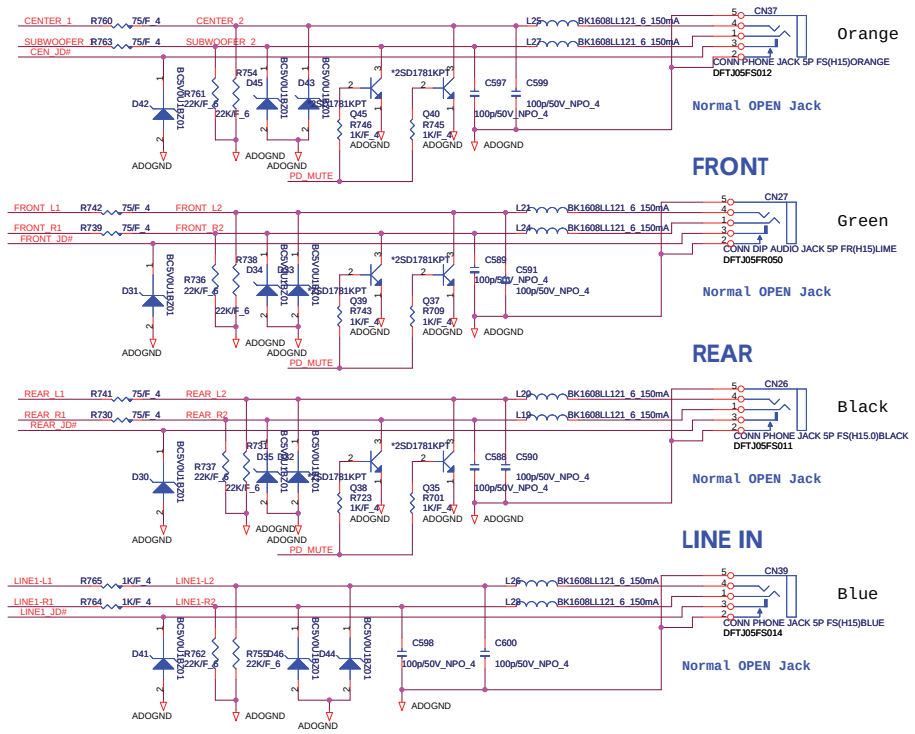
CODEC

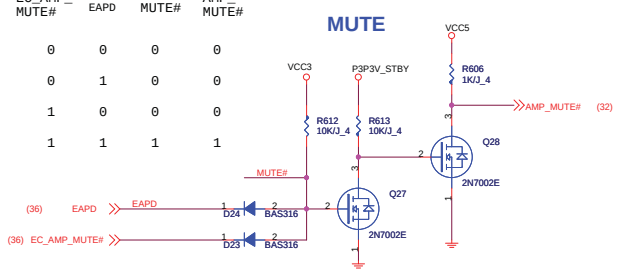


CENTER & SUBWOOFER



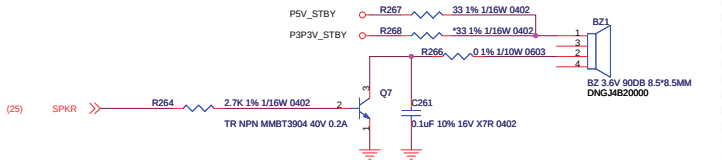
MUTE

EC_AMP_ MUTE#	EAPD	MUTE#	AMP_ MUTE#
0	0	0	0
0	1	0	0
1	0	0	0
1	1	1	1

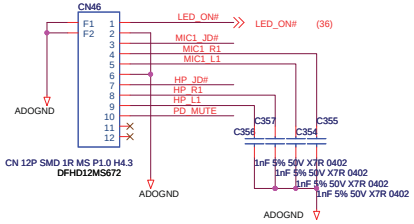


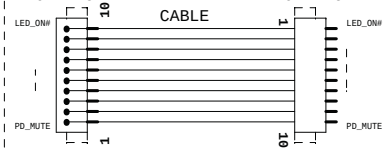
BUZZER

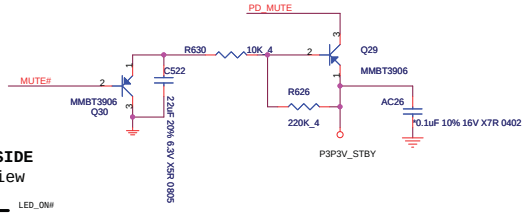
A02



EXT. MIC & HP







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Title	AUDIO CODEC-ALC888/MIC/JACK	
Size C	Document Number EL5	Rev A02
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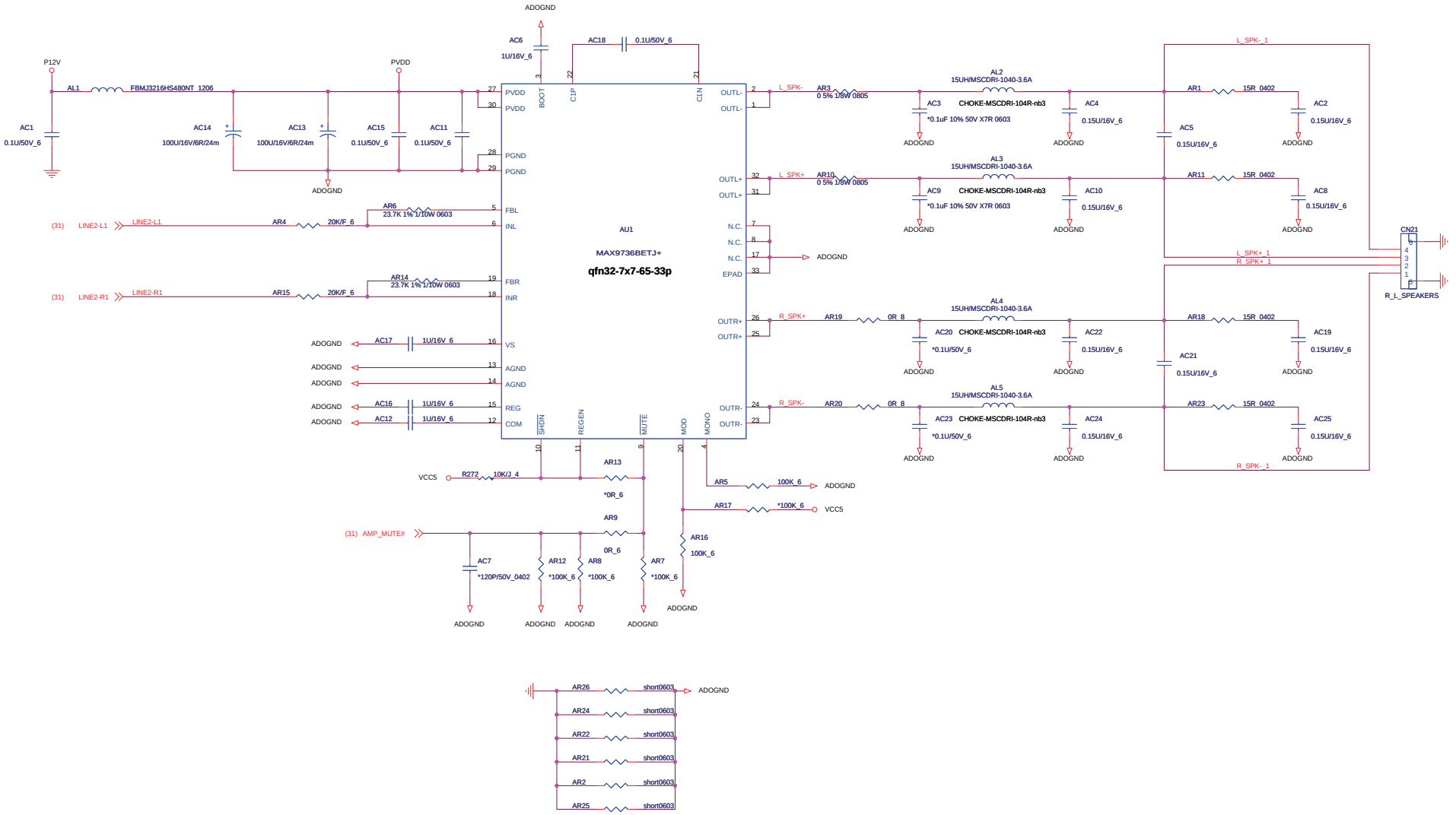
Speaker AMP.



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Title		
	AUDIO AMP	
Size C	Document Number EL5	Rev A02
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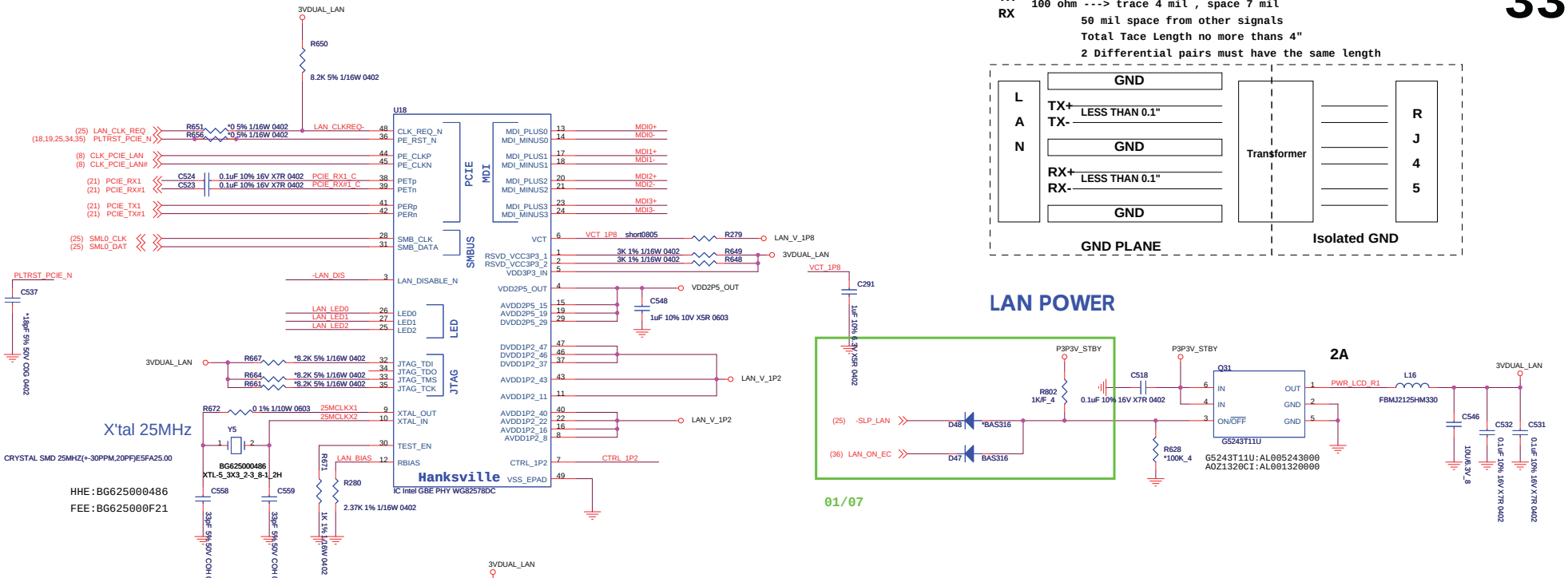
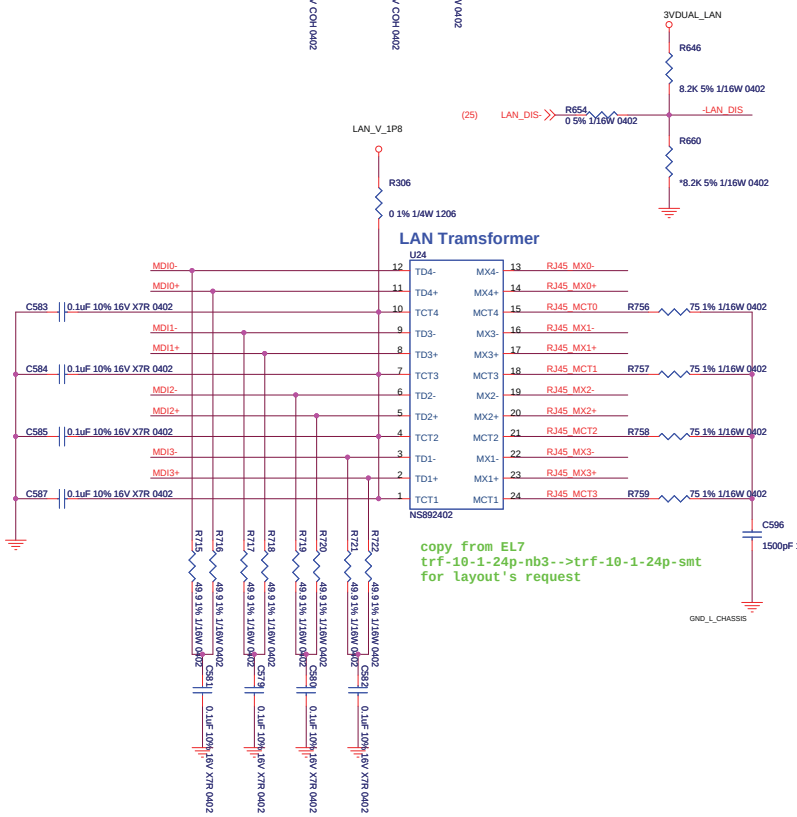
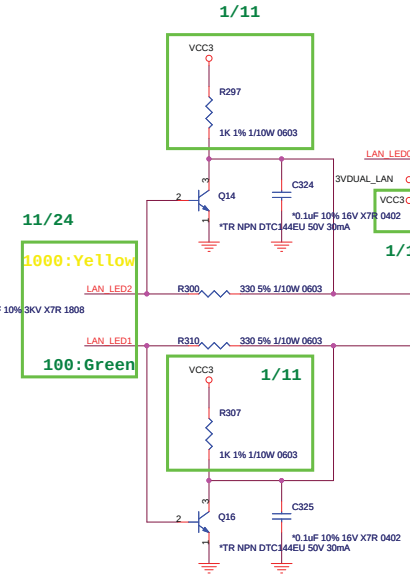
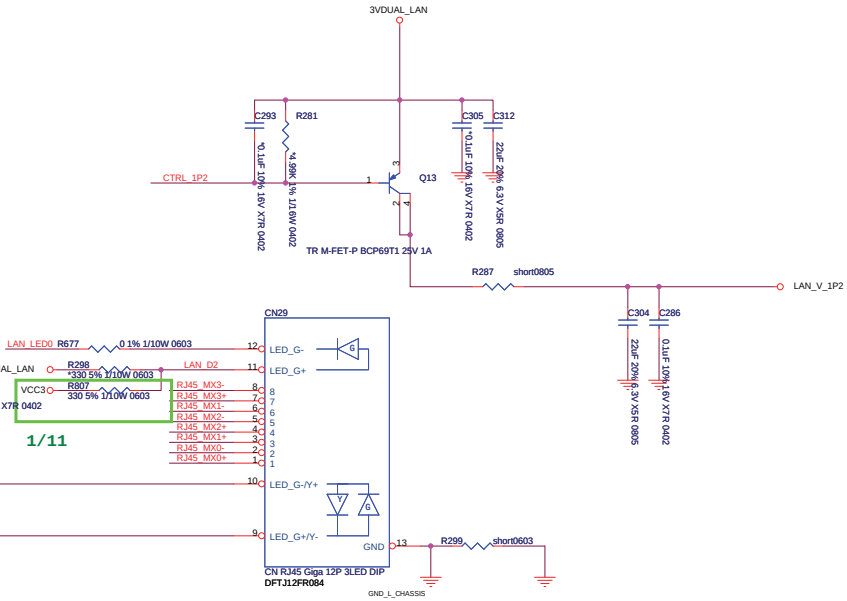
TX
RX
100 ohm ---> trace 4 mil , space 7 mil
50 mil space from other signals
Total Tace Length no more thans 4"
2 Differential pairs must have the same length

LAN POWER









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Title	GBLAN-Intel 82578/RJ45	
Size C	Document Number EL5	Rev A02
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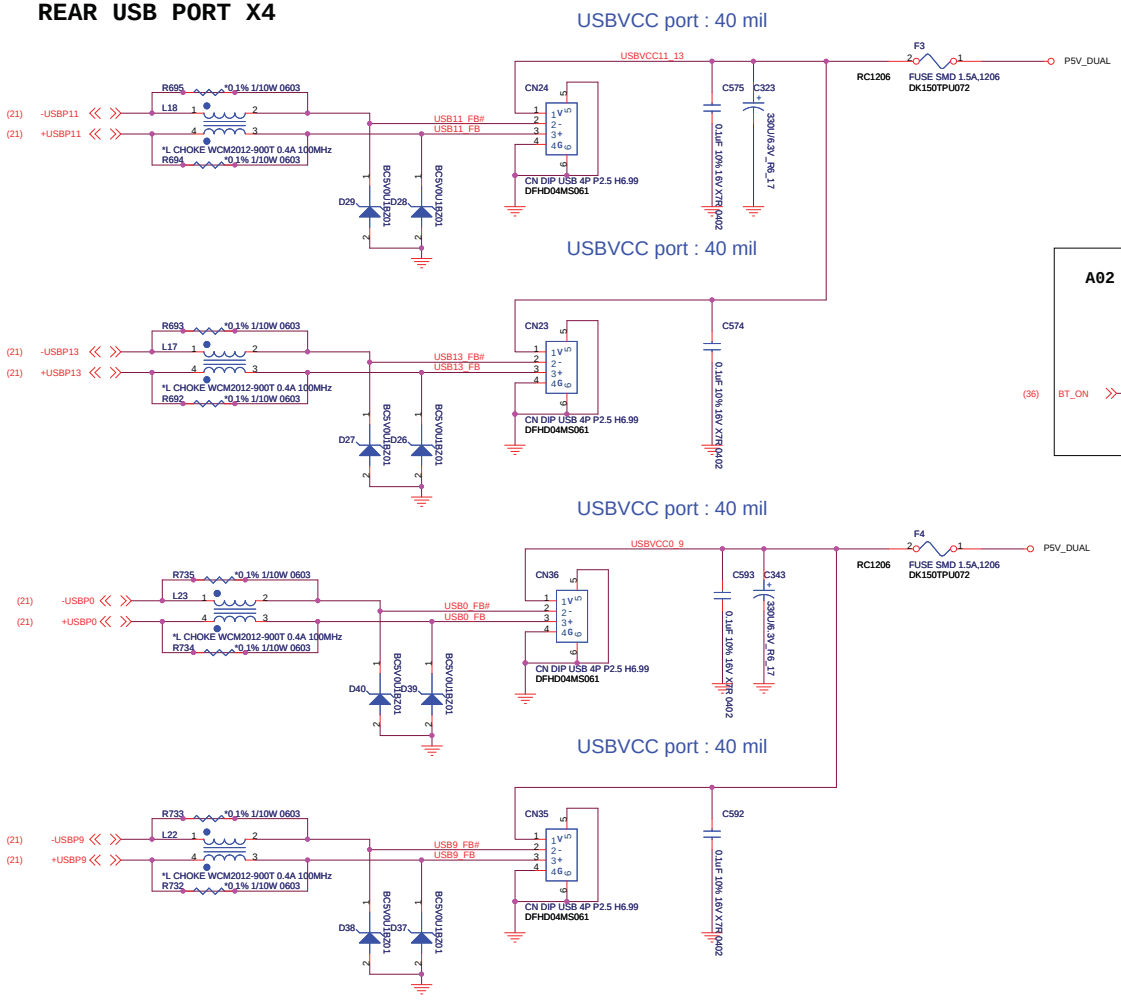
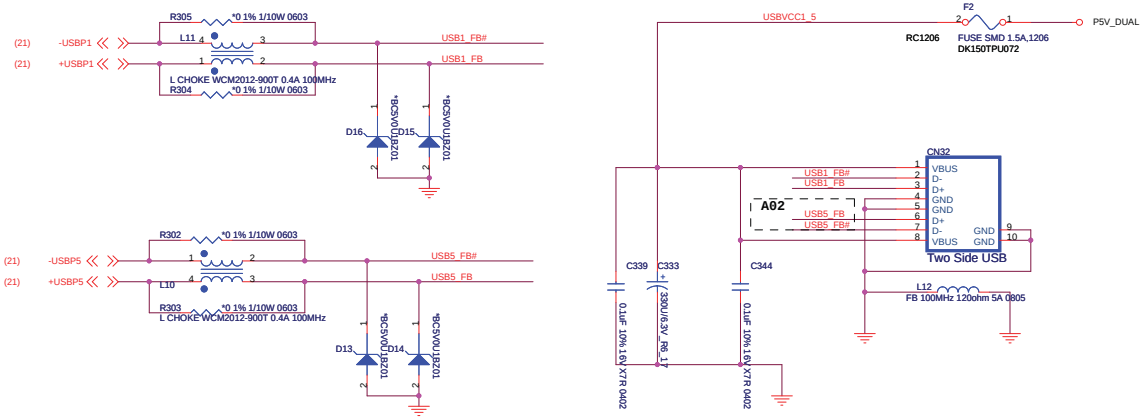
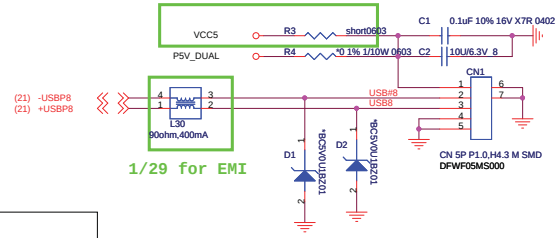
REAR USB PORT X4



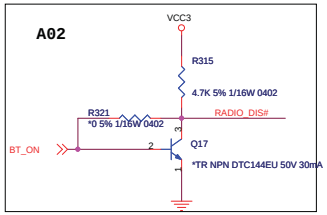
SIDE USB PORT X2



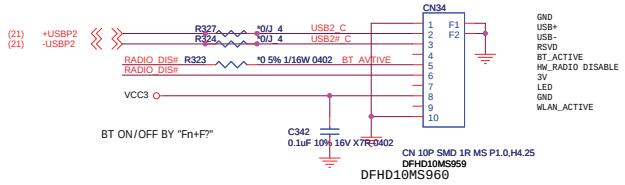
Touch Panel connector



1/29 for EMI

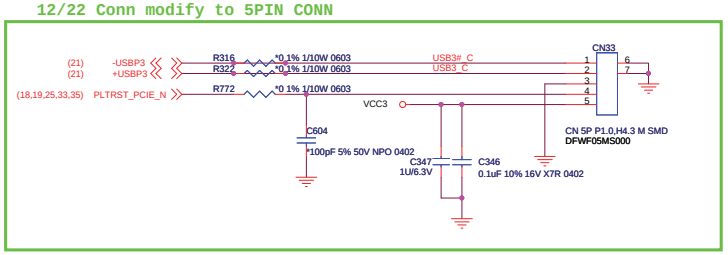


BLUETOOTH connector



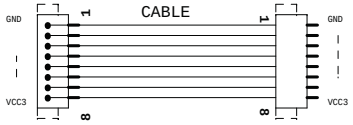
MEDIA READER connector

12/22 Conn modify to 5PIN CONN



M/B Side
TOP View

Card reader/B SIDE
TOP View



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Title	USB PORT/BLUETOOTH/MEDIA READER CNN	
Size C	Document Number EL5	Rev A02
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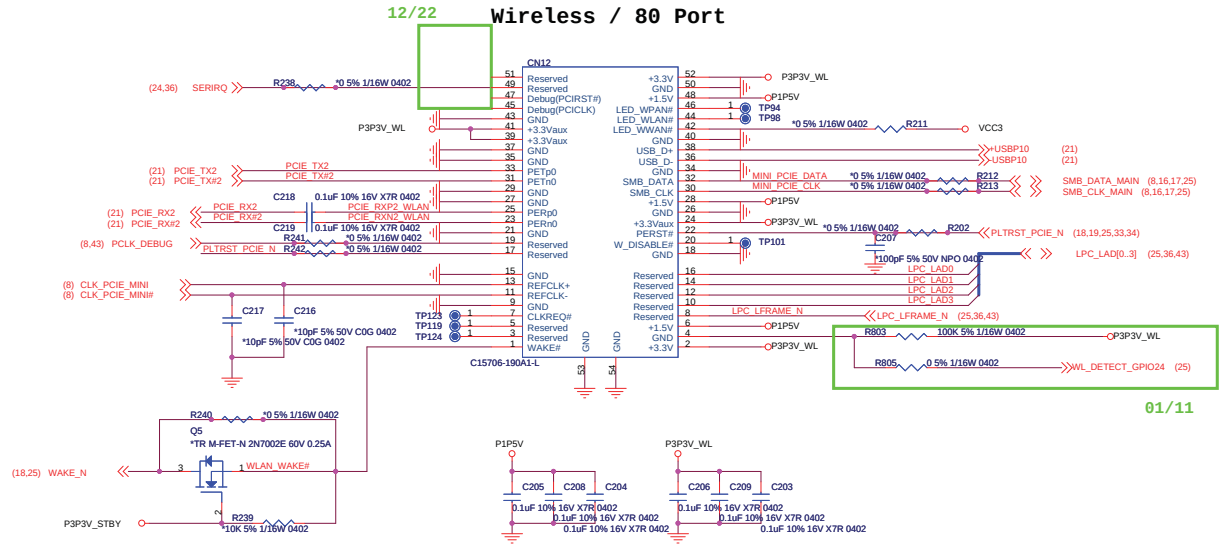
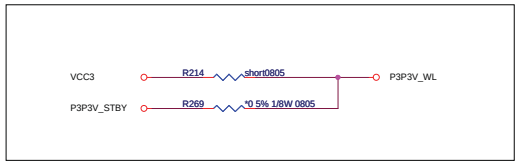
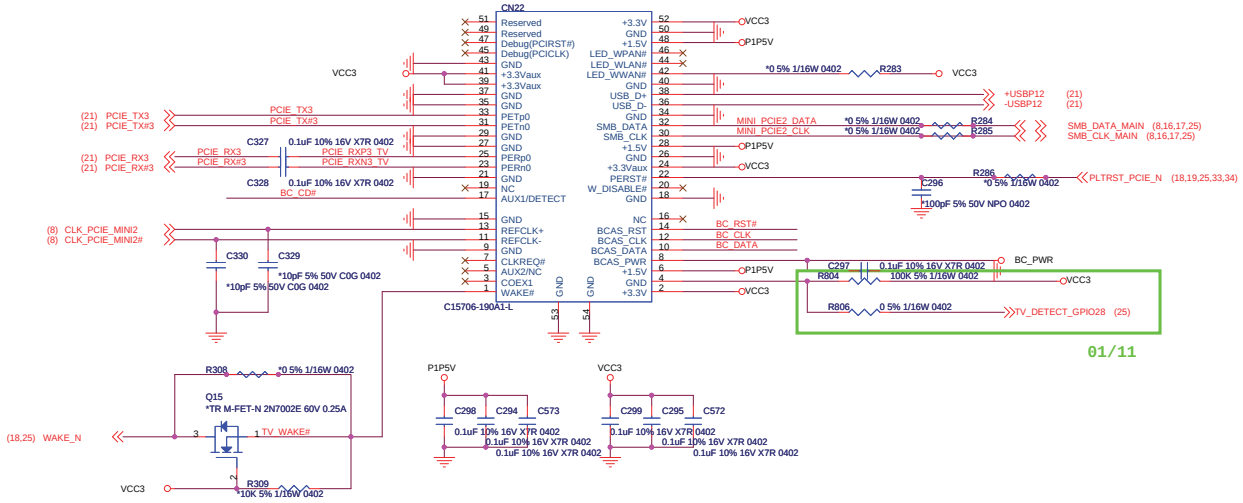
Wireless / 80 Port

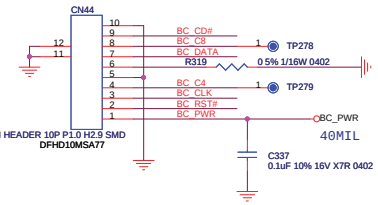




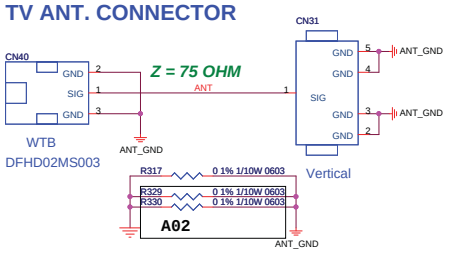
TV Card



B-CAS CONN



TV ANT. CONNECTOR



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Title	MINI PCIE-WLAN/TV, B-CAS CN	
Size C	Document Number EL5	Rev A02
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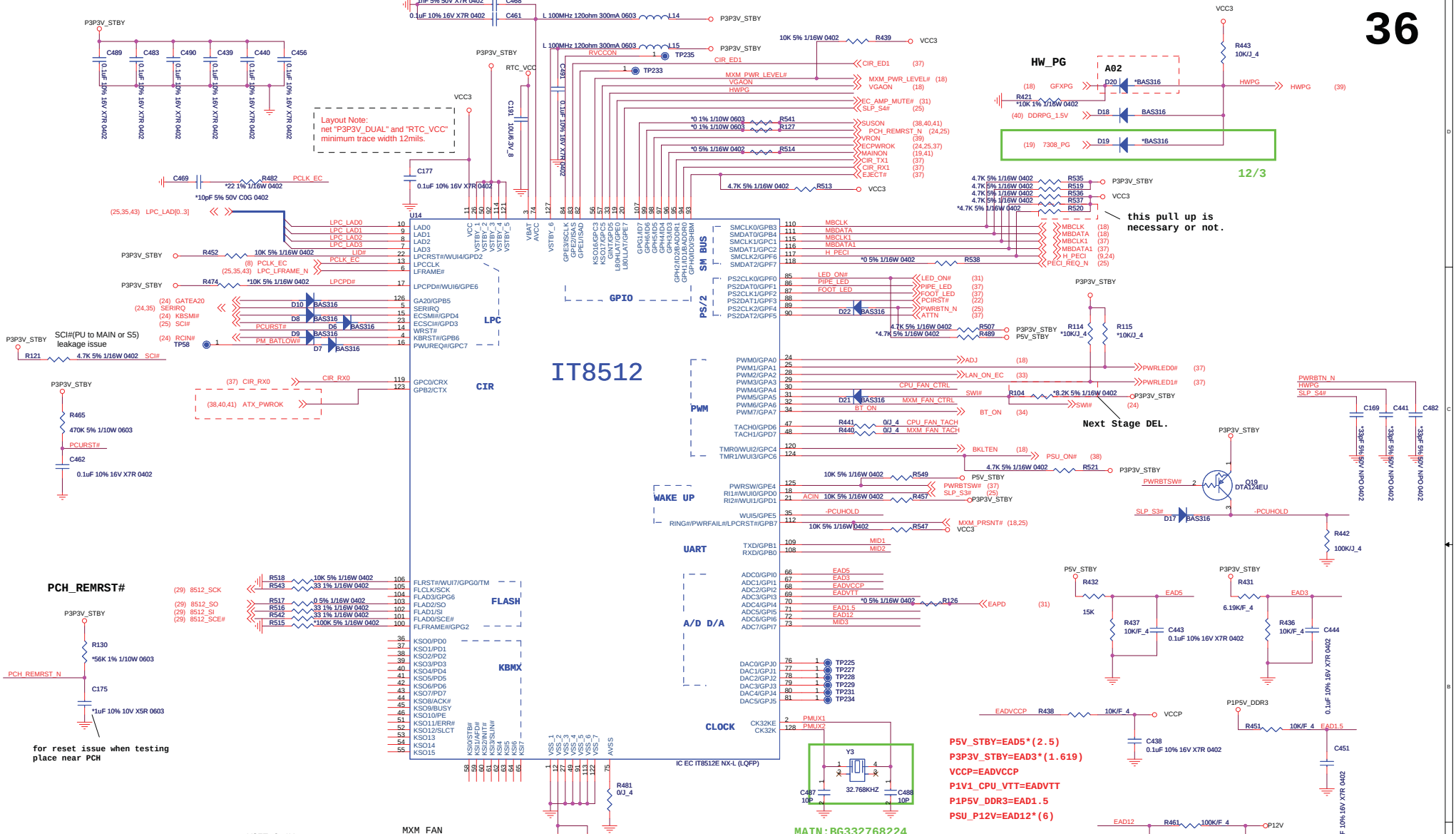
IT8512
IC EC IT8512E NX-L (LQFP)
Layout Note:
net "P3P3V_DUAL" and "RTC_VCC"
minimum trace width 12mils.
HW_PG
A02
12/3
this pull up is
necessary or not.
Next Stage DEL.
SCI#(PU to MAIN or S5)
leakage issue
PCH_REMRST#
for reset issue when testing
place near PCH
P5V_STBY=EAD5*(2.5)
P3P3V_STBY=EAD3*(1.619)
VCCP=EADVCCP
P1V1_CPU_VTT=EADVTT
P1P5V_DDR3=EAD1.5
PSU_P12V=EAD12*(6)
MAIN:BG332768224
Second:BG332768024
CPU FAN
Vout=4*Vset
VSET 3~1V
VSET = 3V ; VO = 12V
VSET = 1V ; VO = 4V
MXM FAN
Vout=4*Vset
GPB1 GPB0
MID1 MID2
1 1 ACER(default)
1 0 Gateway
0 1 Packard Bell
0 0
OFF=1= Hi On= 0= Low
GPI7
MID3
1 OS(default)
0 Free DOS
SW 4x2 NHDS-04F-T-V-T/R SMD
DHDNHDS0400
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211, Wen Hwa 2nd Rd., Kuei Shan,
Tao Yuan 33377, Taiwan
Tel : +886-3-327-2345
Title
EC-ITE8512/FLASH ROM/FAN CN
Size C
Document Number EL5
Rev A02
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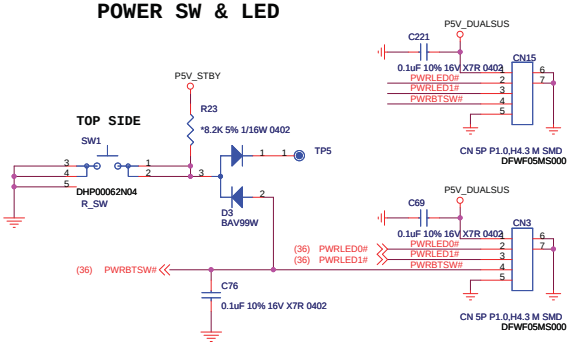
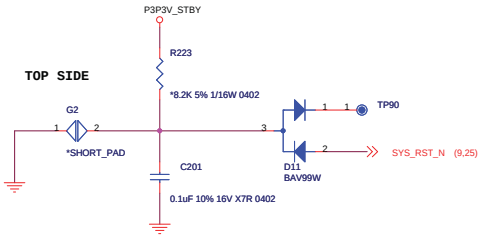
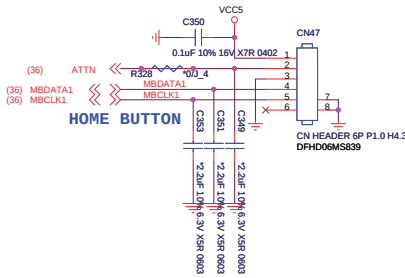
POWER SW & LED



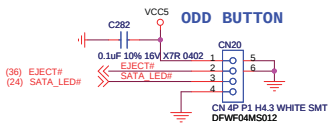
SYSTEM RESET



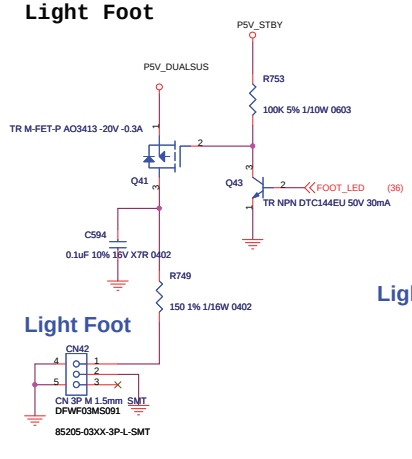
HOME BUTTON



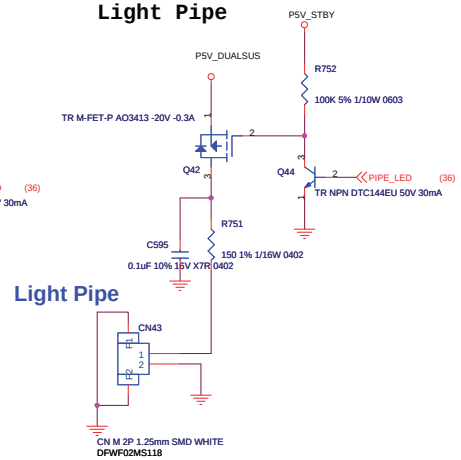
ODD EJECT



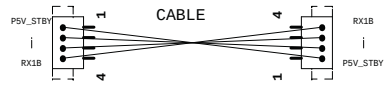
Light Foot



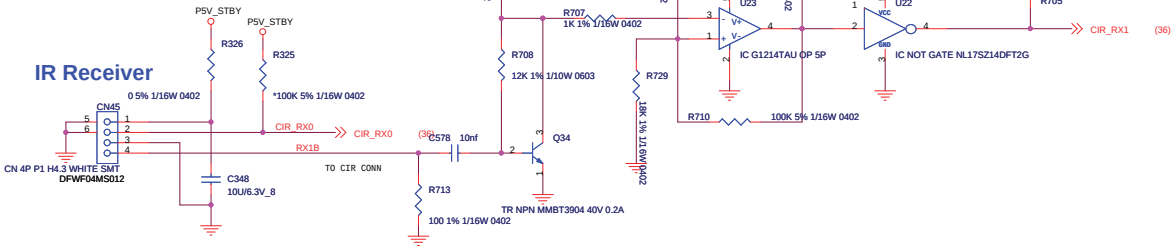
Light Pipe



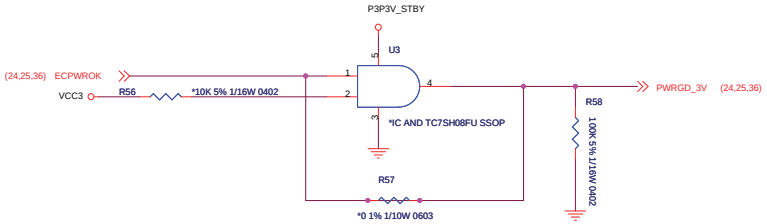
M/B Side TOP View — IR/B SIDE TOP View



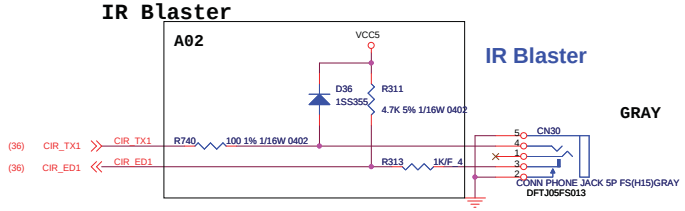
IR Receiver



PCH POWEROK



IR Blaster



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Title	POWER SW/FRONT PANEL CN/IR	
Size C	Document Number EL5	Rev A02
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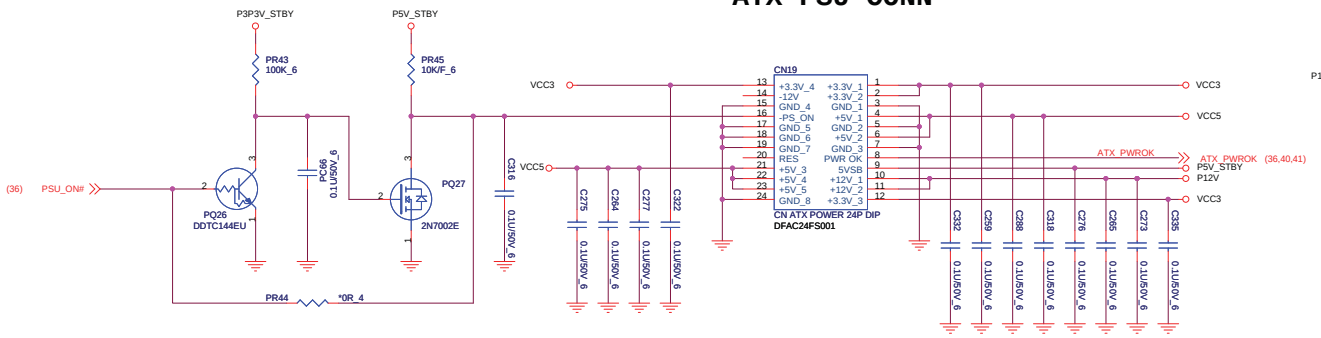
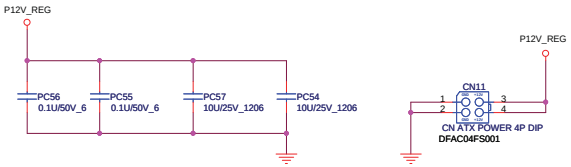
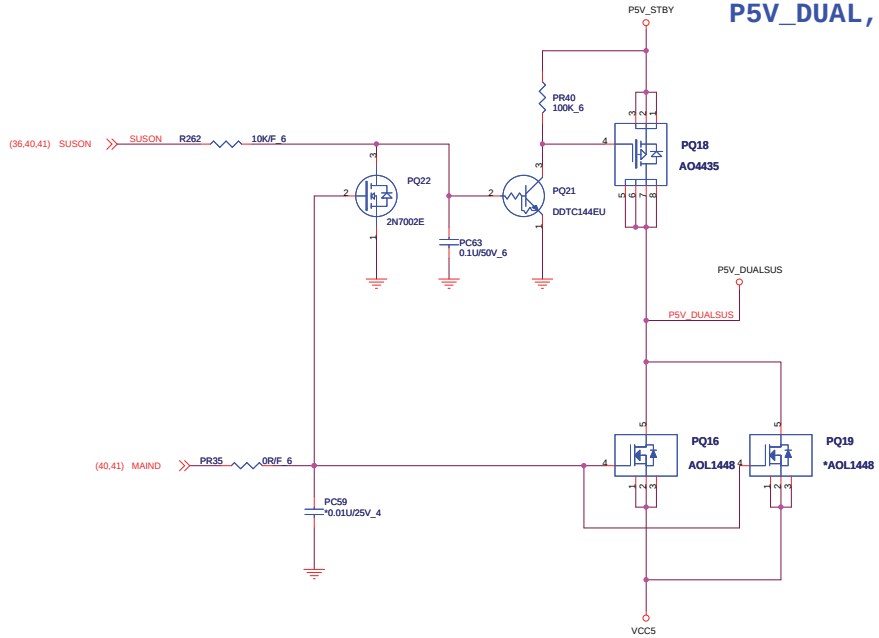
ATX PSU CONN

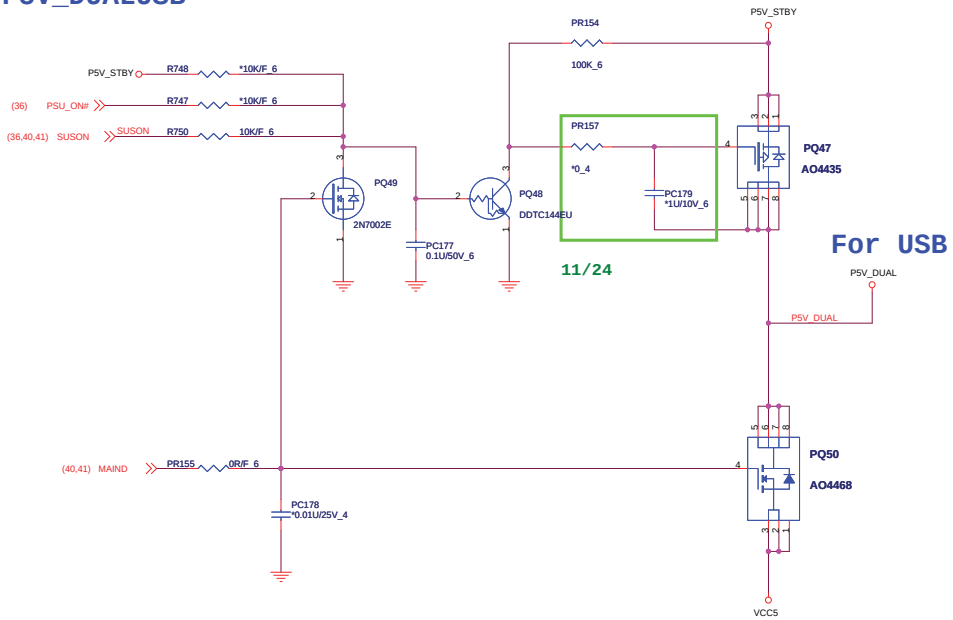


4PIN +12V_REG for CPU_CORE

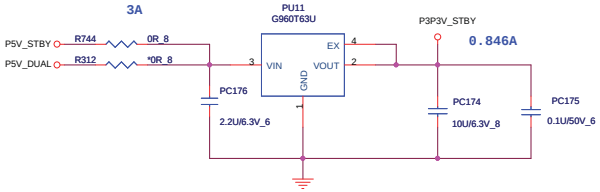


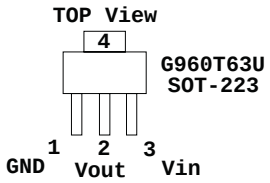
P5V_DUAL, P5V_DUALUSB





For EC&LAN





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Title	PSU, 3V/5V DUAL	
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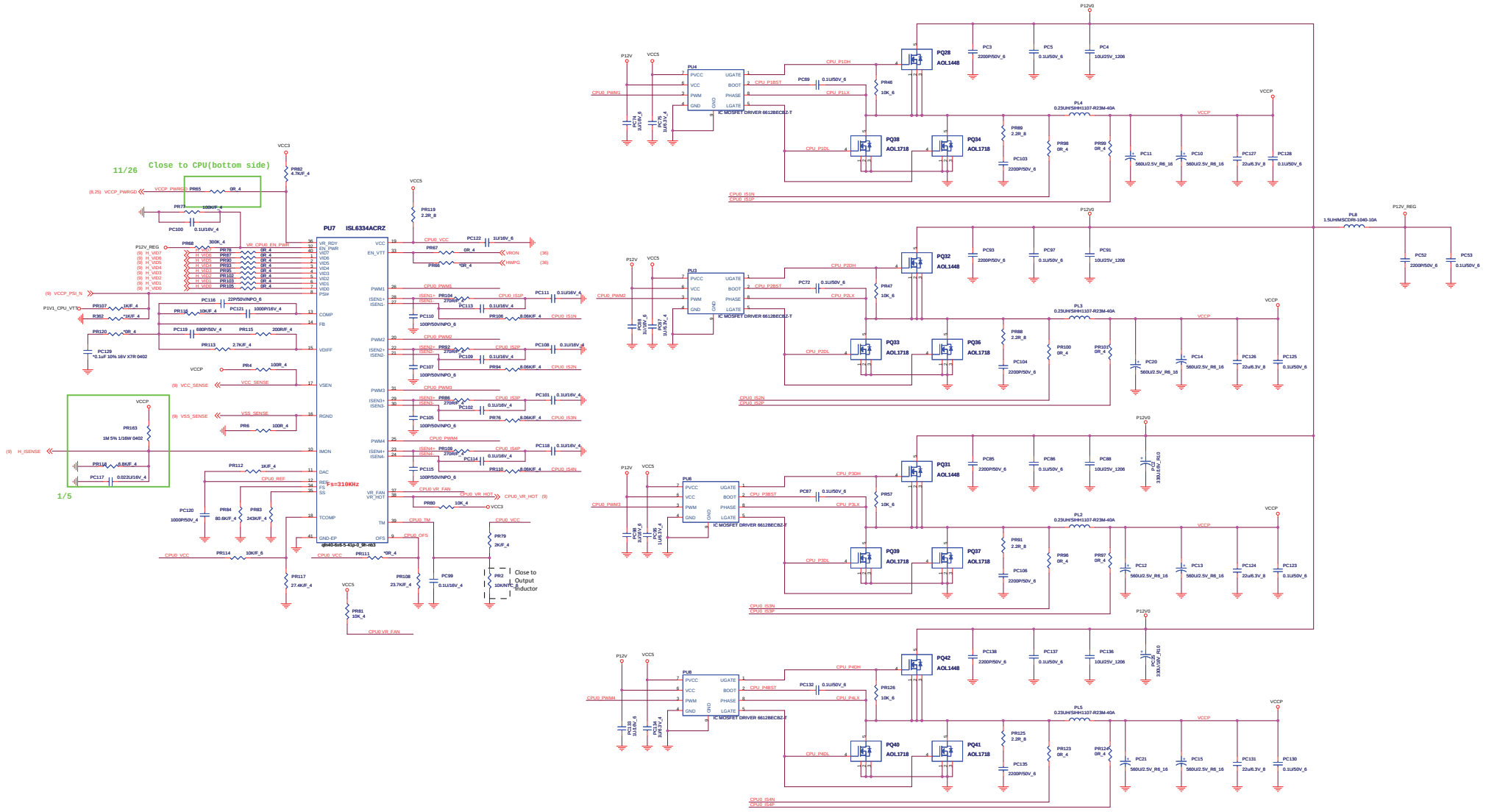

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Title	CPU CORE-VRM11.1	
Size D	Document Number EL5	Rev A02
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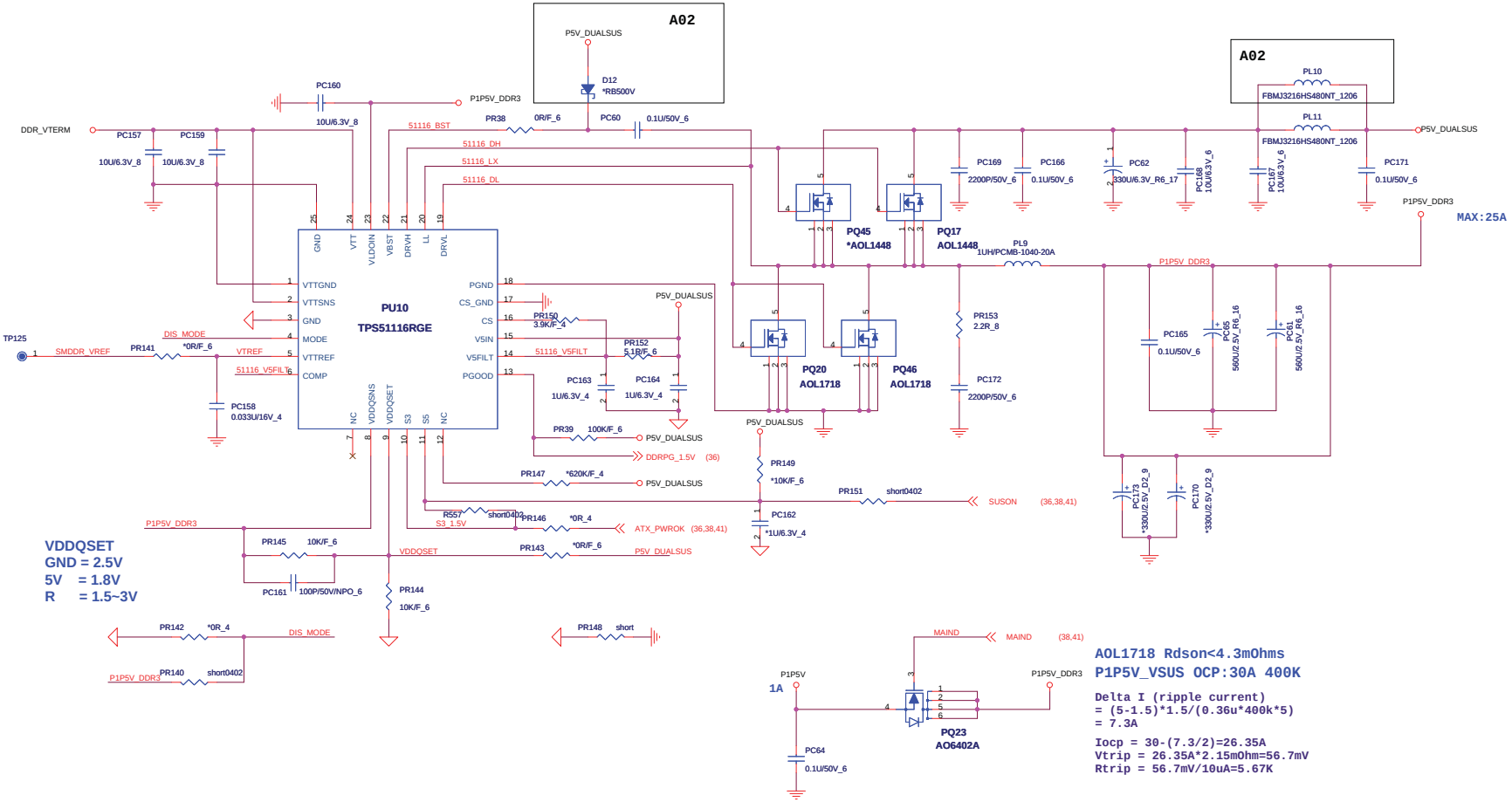
DDRIII P1P5V_SUS (TPS51116)



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Title		
DDRIII POWER-1.5VSUS		
Size C	Document Number EL5	Rev A02
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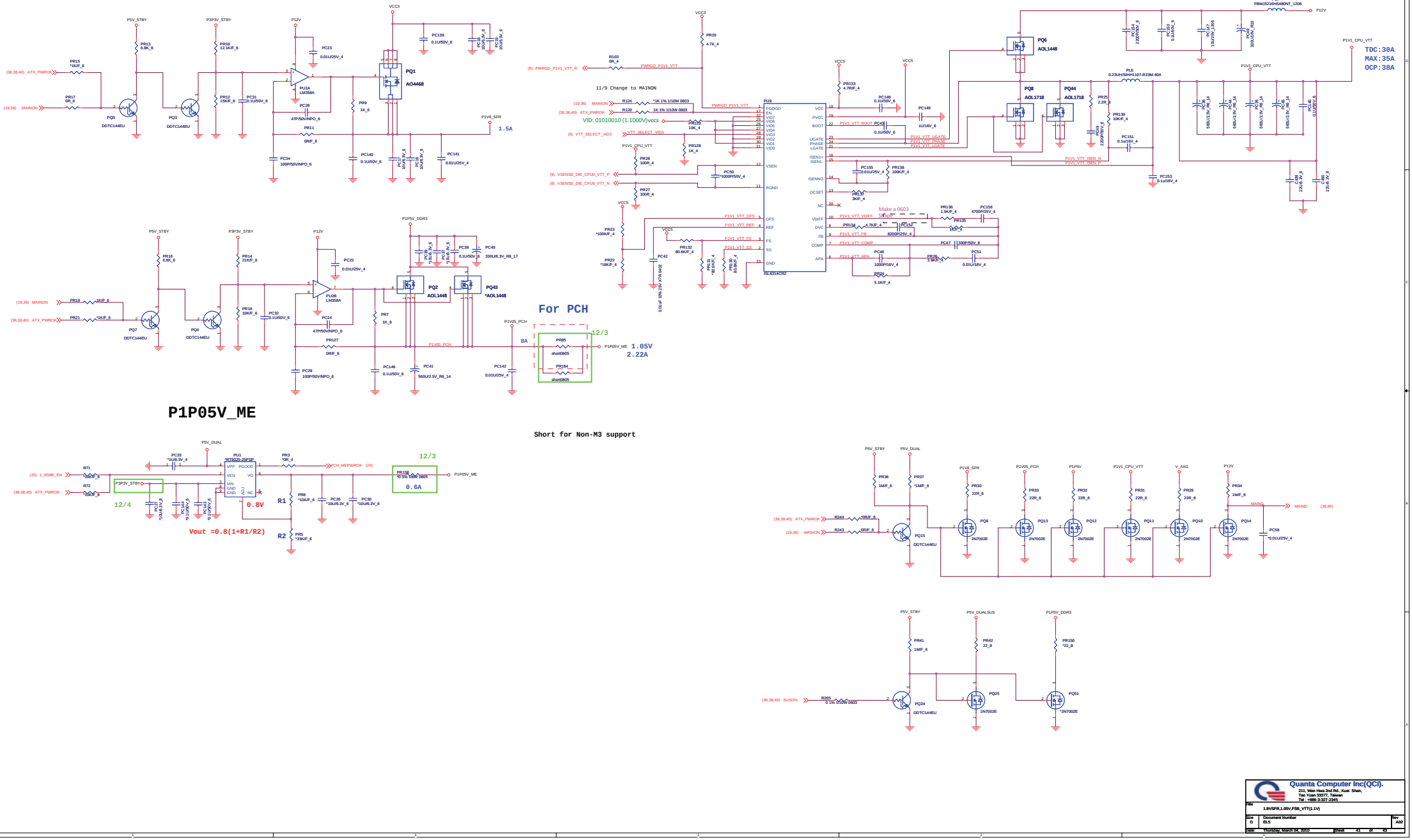
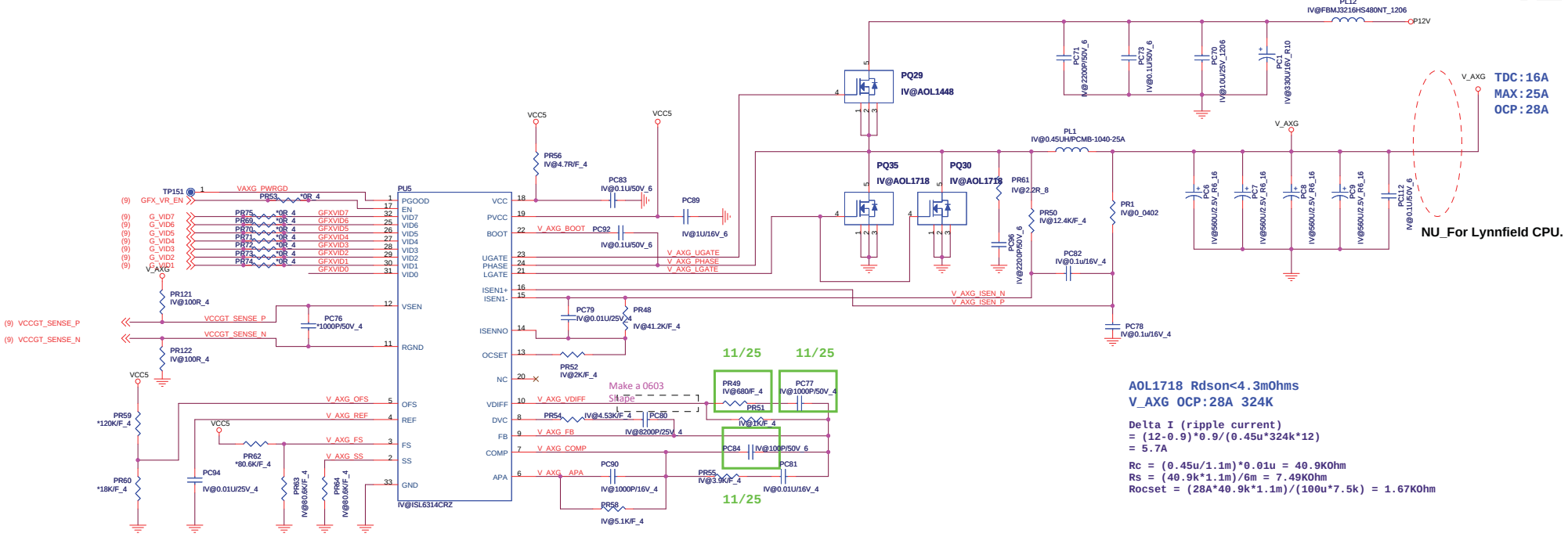
V_1P8_SRF, P1P05V_PCH



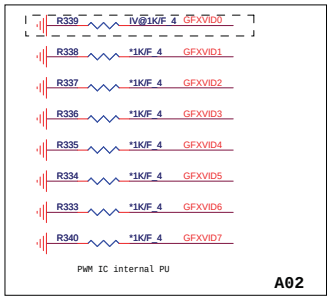
V_AXG



AOL1718 Rdson<4.3mOhms
V_AXG OCP:28A 324K

Delta I (ripple current)
= (12-0.9)*0.9/(0.45u*324k*12)
= 5.7A

Rc = (0.45u/1.1m)*0.01u = 40.9KOhm
Rs = (40.9k*1.1m)/6m = 7.49KOhm
Rocset = (28A*40.9k*1.1m)/(100u*7.5k) = 1.67KOhm



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Title		
GFX_VCC		
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02/22 Change size for ME

01/08 Add PAD FOR EMI

H11 H-C67D67N
H13 H-C87D87N
H4 H-C87D87N
PAD1 SPAD-RE1175X985NP
SPAD-RE1175X985NP
H25 H-EL5_MB-1
H26 H-EL5_MB-1
H-EL5_MB-1
H-EL5_MB-1

H23 H-C322D217P2
H22 H-C322D217P2
H8 H-C322D217P2
H9 H-C322D217P2
H16 H-TC472BC276D110P2
H10 H-TC472BC276D110P2

H15 H-C276D138P2
H12 H-C276D138P2
H19 H-C276D138P2
H21 H-C217D124P2
H14 H-C217D124P2

H18 H-C276D118P2
H5 H-C276D118P2
H31 H-O-EL5-1
ADOGND
H32 H-O-EL5-1

12/22

H29 H-C276D157P2
H30 H-C276D110P2
H1 H-C276D110P2
H33 O-EL5-2
H6 H-C1575D1575N
H7 H-C1969D1969N

H28 h-c276d110p2
H24 H-c355d110p2
H2 H-C276D157P2
H3 H-C276D110P2
H17 H-TC236D130P2
H20 H-TC236D130P2
H27 H-TC236D130P2

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WLAN / TV

VCC3	C313	*0.1uF 10% 50V X7R 0603		
VCC3	C249	*0.1uF 10% 50V X7R 0603	P1P5V_DDR3	
	C165	*0.1uF 10% 50V X7R 0603		
VCC3	C326	*0.1uF 10% 50V X7R 0603		
	C119	*0.1uF 10% 50V X7R 0603		
VCC3	C274	*0.1uF 10% 50V X7R 0603	P1P5V_DDR3	
VCC3	C82	*0.1uF 10% 50V X7R 0603	P12V	
VCC5	C23	*0.1uF 10% 50V X7R 0603	P12V	
	C20	*0.1uF 10% 50V X7R 0603		
P12V0	C358	*0.1uF 10% 50V X7R 0603	P12V	
P12V0	C367	*0.1uF 10% 50V X7R 0603	VCCP	
V_AXG	C78	*0.1uF 10% 50V X7R 0603	VCCP	
V_AXG	C79	*0.1uF 10% 50V X7R 0603		
ADOGND	C336	*0.1uF 10% 50V X7R 0603		
ADOGND	C320	*0.1uF 10% 50V X7R 0603	VCC3	
	C317	*0.1uF 10% 50V X7R 0603		
P5V_DUAL	C222	*0.1uF 10% 50V X7R 0603	P1P5V_DDR3	
P5V_DUAL	C215	*0.1uF 10% 50V X7R 0603	P12V	
P1V1_CPU_VTT	C176	*0.1uF 10% 50V X7R 0603		
P1V1_CPU_VTT	C392	*0.1uF 10% 50V X7R 0603	VCCP	

VCC3	C618	0.1uF 10% 50V X7R 0603	
VCC3	C619	0.1uF 10% 50V X7R 0603	
VCC3	C620	0.1uF 10% 50V X7R 0603	
VCC3	C621	0.1uF 10% 50V X7R 0603	
VCC3	C622	0.1uF 10% 50V X7R 0603	
VCC3	C623	0.1uF 10% 50V X7R 0603	
VCC3	C624	0.1uF 10% 50V X7R 0603	
VCC3	C625	0.1uF 10% 50V X7R 0603	ADOGND
VCC3	C626	0.1uF 10% 50V X7R 0603	ADOGND
VCC3	C627	0.1uF 10% 50V X7R 0603	ADOGND
VCC3	C628	0.1uF 10% 50V X7R 0603	ADOGND
VCC3	C629	0.1uF 10% 50V X7R 0603	P1P5V_DDR3

2/23 For EMI

CONN(LPC Debug Card)

(25,35,36) LPC_LAD[0..3]
LPC_LAD3
LPC_LAD2
LPC_LAD1
LPC_LAD0
(25,35,36) LPC_LFRAME_N
(8,35) PCLK_DEBUG
P3P3V_STBY
CN16
1 2 3 4 5 6 7 8 9 10
*CN HEADER 8P P1.0 H4.3 SMD
DFHD08MS036

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